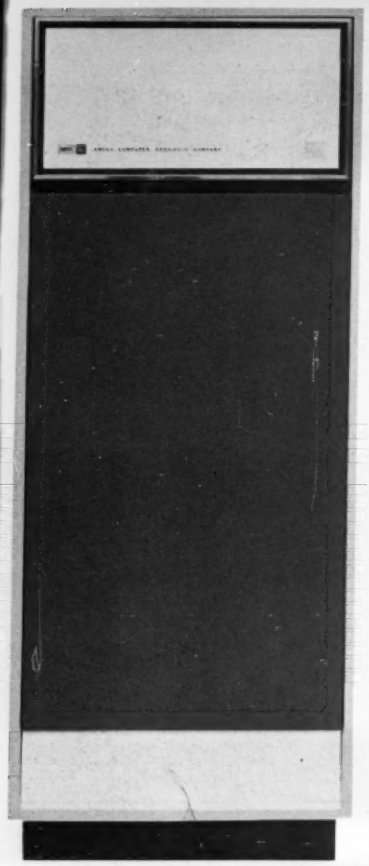
DATAMATION 61

May

Dr Herb Grosch
415 E 52nd St
New York 22 N Y
25

DESIGN TRENDS FOR LARGE COMPUTER SYSTEMS



THIS MEMORY IS 25% FASTER!

Access time just 2μ seconds (2.5 in previous models). Memory cycle a speedy 5μ seconds. Buffer operation 2.5μ seconds. That's the new RQA, and it stores up to 32,768 sixty bit words for random access applications and high speed sequential buffer operations. Sound like something you'd care to know more about? Send for our 8-page operations and specifications brochure to get the complete story: Ampex Computer Products Company, P.O. Box 329, Culver City, California.

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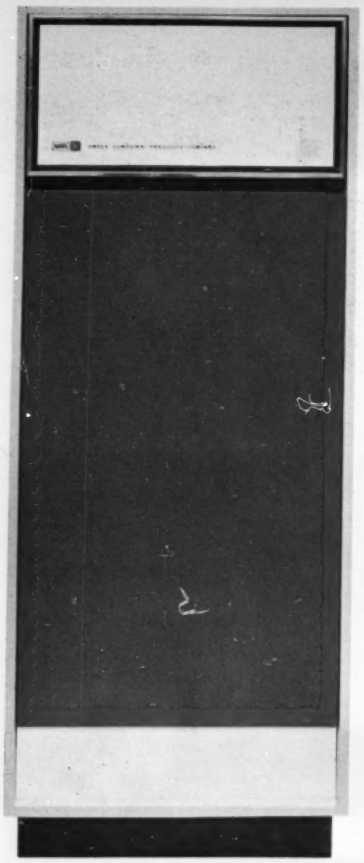

THIS MEMORY USES 50% LESS POWER!

4,096 sixty bit words need a power input of only 1.2 kw (previous models required 2.5). And the new RQA operates over a much wider temperature range as well. Remember the old spread: +15° to +35°C? The new RQA does 350% better, at a range of −10° to +60°C. Might be wise to send for the detailed operations and specifications booklet right now, while you're thinking about it. Ampex Computer Products Company, P.O. Box 329, Culver City, California.

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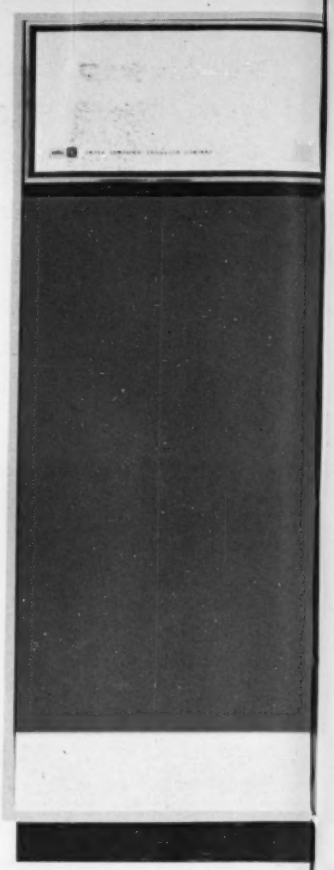

THIS MEMOR IS 75% SMALLE

Occupies less than 3.5 sq. ft. floor space (as opposed to 6.0 previous models). It stands mere 52 inches high. This co pact beauty is modular, too. you need a larger word capacit Just add as many 8,192 wo units as you like (up to 32,7 sixty bit words, that is). Bet write for the 8-page operatio and specifications pamph today. It'll help you remem our memory better. Ampex Co puter Products Company, P Box 329, Culver City, Californ

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CIRCLE 1 ON READER CARD

Scientific programmers for **S**pace **T**echnology **L**eadership

*"And, thinking it would not be improper, I have . . . plotted in the plane of the curve, a true representation of the orbit which this comet (Halley's) described . . ." Isaac Newton—"Mathematical Principles of Natural Philosophy—*BOOK III: *The Systems of the World," 1687*

REPRINTS OF THE DRAWINGS CREATED FOR THIS SERIES, SUITABLE FOR FRAMING, ARE AVAILABLE ON REQUEST.

Thinking it not improper, we invite your attention to the challenging opportunities for scientific programmers at Space Technology Laboratories, Inc. In the tradition of Newton, you might well be interested in helping to develop a better understanding of such phenomena as the orbiting of bodies—celestial and man-made. At STL there is continuing interest in the solution of the broad spectrum of unsolved problems relating to space technology. It is indeed proper, therefore, that we invite you to participate with us in exploring new areas of Space Technology Leadership. Your inquiry will be welcomed and will receive our meticulous attention.

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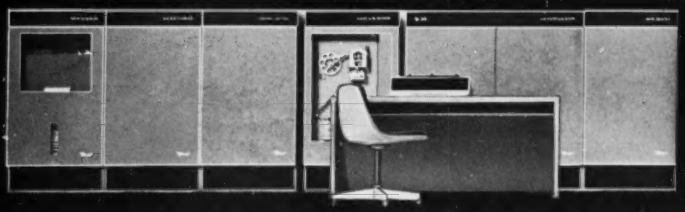
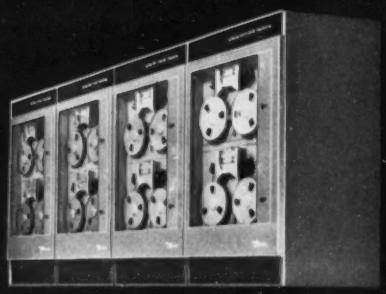
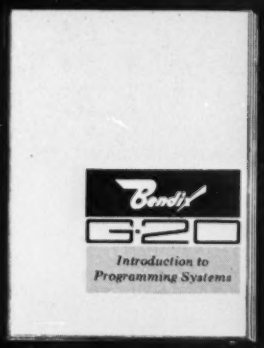
BENDIX
G-20 COMPUTER
'SPACE'
PROGRAMMING







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CIRCLE 4 ON READER CARD

DATAMATION 61

the automatic handling of information

volume 7, number **5**

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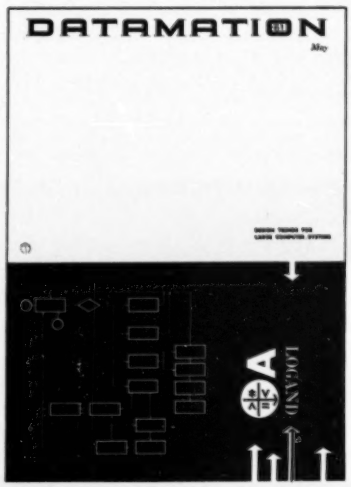

Cover

The emphasis on programming in today's large computer systems is symbolized by this month's cover design. Three such systems — the ATLAS, B 5000, and AN/UYK-1 — receive major feature treatment in this issue.

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Recomp III is the *only* low-priced computer that offers you built-in compacted floating point hardware and the new Facitape high speed paper tape reader and punch as optional features.

Now you can get Recomp's proven performance and quality for *no* more than you pay for lesser computers... and it is now available.

If your computer problems have grown and your computer hasn't; if you need a small-scale digital computer; now, for a lease price equal to what you are already paying or would expect to pay for an outdated computer, you can have the newest, most advanced, small-scale computer on the market—Recomp III.

For a convenient do-it-yourself comparison of Recomp III with your present computer or a competitive computer see the following page.

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	RECOMP III	COMPETITIVE COMPUTER
Monthly lease price	$1,495.00	$_____
Input Standard	Mechanical Reader	_____
	10 char/sec	_____
	Typewriter Engineering Keyboard	_____
	Typing Speed	_____
	Full Alphanumeric Input	_____
Input Optional	Capacitance Reader	_____
	600 char/sec (stops within a char)	_____
	Up to any type of four inputs	_____
Arithmetic Speeds—Fixed Point		
Add & subtract	.54 milsec (12 digits)	_____
Multiply	10.8 milsec (12 digits)	_____
Divide	11.3 milsec (12 digits)	_____
Access Time—Main Memory—average	9.0 milsec	_____
High Speed Loops—average	1.7 milsec	_____
Arithmetic Speeds—Floating Point		
Add & subtract	.81 milsec (12 digits)	_____
Multiply	8.6 milsec (12 digits)	_____
Divide	8.9 milsec (12 digits)	_____

	RECOMP III	COMPETITIVE COMPUTER
Memory	Disk—Non-volatile	_____
	Capacity 4096 words	_____
	Word size 40 bits & sign	_____
	12 decimal digits	_____
	Command size—2 commands per word	_____
	Instruction capacity 8192 instructions	_____
Programming	Machine language (fixed point) very simple and versatile	_____
	Machine language (floating point) very simple and versatile	_____
Outputs—Standard	Typewriter (alphanumeric engineering keyboard)	_____
	10 char/sec (printing speed)	_____
	Paper Tape Punch	_____
	10 char/sec (punching speed)	_____
Outputs—Optional	Facitape High Speed Punch	_____
	150 char/sec	_____
	Up to four outputs	_____
Characteristics	250 pounds (computer)	_____
	Solid State	_____
	Desk size	_____
Power Requirements	3.5 amps any wall outlet 115 v ac	_____
Heat	No cooling needed	_____

If your computer, or a competitive computer, doesn't measure up to Recomp III, this coupon can save you time and money.

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CIRCLE 5 ON READER CARD

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It is simple to program and operate, so no special programmer is needed. An engineer can use it himself. It requires no air-conditioning or costly installation. It plugs into any 110-volt AC wall outlet. It is mobile, so it rolls anywhere. It is desk-size, so it requires little room.

This means that the Royal Precision LGP-30 is ready to go to work to help your company create new products—and fresh profits—the very same day it is delivered. Can you wonder that there are more LGP-30's installed and working right this minute than any other electronic computing system in its class?

For more information: write Floyd Ritchie, Royal McBee Corporation, Port Chester, New York.

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ROYAL McBEE | GENERAL PRECISION

ELECTRONIC DATA PROCESSING SYSTEMS

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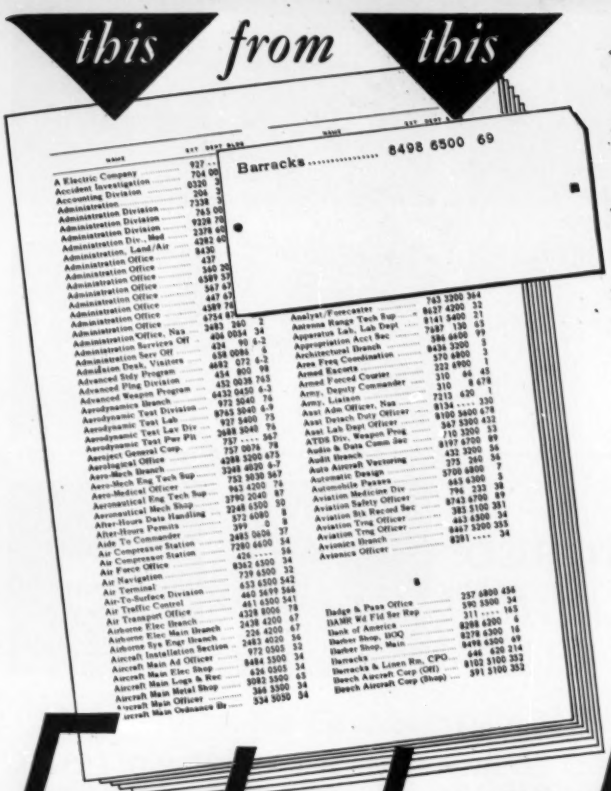


← automatically

← direct from your files

← without typesetting

← without error

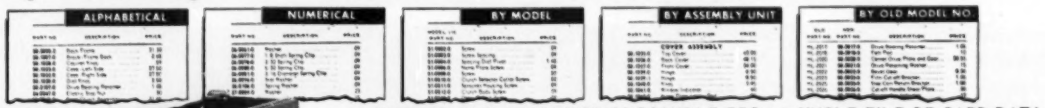
The FOTOLIST System will automatically process the information on your file cards into perfectly aligned and uniformly spaced listings, producing a ready-for-plate negative at the same time. Exclusive registering mechanisms insure hairline accuracy of column alignment and line spacing despite the machine's high speed. The data on the original cards is recorded on a VARITYPER machine with any combination of printer's style and size of type *(instantly changeable)*. Thus, the finished listing will have all the attractiveness and legibility of professional metal type composition while completely eliminating its cost, time and proofreading.

The VARITYPER Machine wrote the text for this advertisement. The headlines were photocomposed on the HEADLINER Machine, another office type-composing model

FotoList SYSTEM

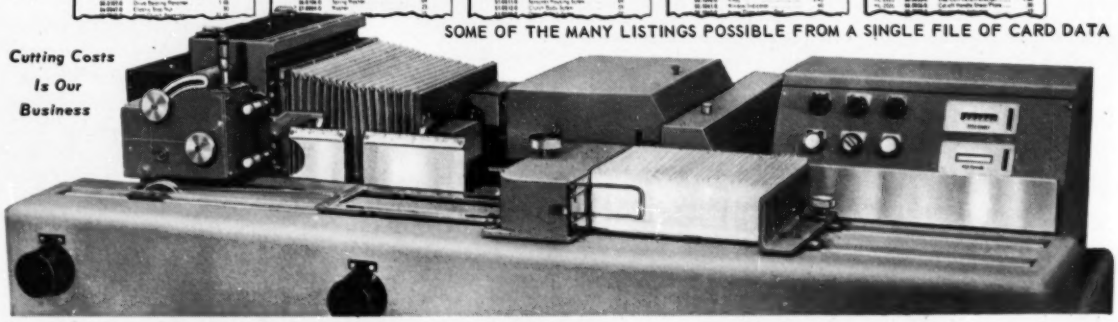
Automatically COMPOSES THE DATA ON YOUR FILE CARDS INTO LISTS, COLUMNS OR PARAGRAPHS OF READING MATTER

...for Catalogs, Directories, Indexes, Parts and Price Books, etc.



SOME OF THE MANY LISTINGS POSSIBLE FROM A SINGLE FILE OF CARD DATA

Cutting Costs Is Our Business



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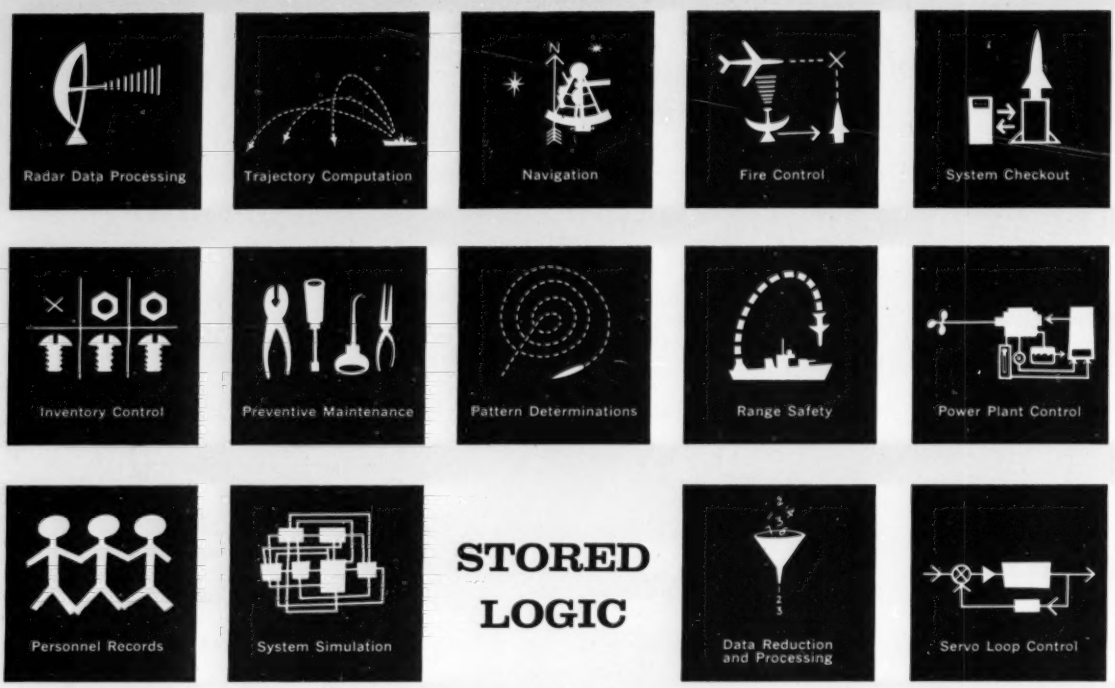

How to get a computer to think it's a one-man gang

Most computers are pretty fussy about the kind of problems they are willing to handle. While it's true that a "business" computer can be made to do "scientific" problems, and vice versa, every experienced computer user knows it's no simple matter to get a machine to accept such a change of character gracefully. Besides the fancy reprogramming involved, the computer is likely to be inefficient and uneconomical at solving problems it wasn't designed for.

From the user's point of view, the "ideal" computer is a *multiple-purpose* machine that can be used *efficiently* in many different types of applications, and at no higher cost than a computer intended primarily for any one of these applications.

From the programmer's point of view, the "ideal" machine is one with a flexible set of instructions that can be easily manipulated to fit just about any kind of problem that comes along. Both programmer and designer are likely to agree that the most practical way to realize this "ideal" computer is by using the *stored logic* principle.

Stored logic concepts developed by Ramo-Wooldridge are being used in the AN/UYK-1, a low-price, multiple-purpose Navy computer intended for shipboard use. In the Ramo-Wooldridge approach, stored logic permits the user to select a word length, order structure and instruction repertoire especially suited to the problem at hand. These normally "wired in" characteristics are specified by data stored in the computer's memory and may be changed during the normal loading procedure without hardware modification.

The AN/UYK-1 "Stored Logic" Multiple-Purpose Computer takes its place alongside the RW-400 "Polymorphic" data processing system as an outstanding example of the kind of advanced work in computer design which has characterized Ramo-Wooldridge over the past six years. Senior programmers are urgently needed to help develop a large "software" package for commercial and military applications of R-W *stored logic* computers, to prepare programs for the polymorphic data processing system, and to work on challenging applications engineering problems. If you are qualified and interested in a career position in this field, contact Mr. Frank Nagel at

AN/UYK-1 "Stored Logic" Multiple-Purpose Computer

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A DIVISION OF

THOMPSON RAMO WOOLDRIDGE INC.

8433 FALLBROOK AVENUE · CANOGA PARK, CALIFORNIA

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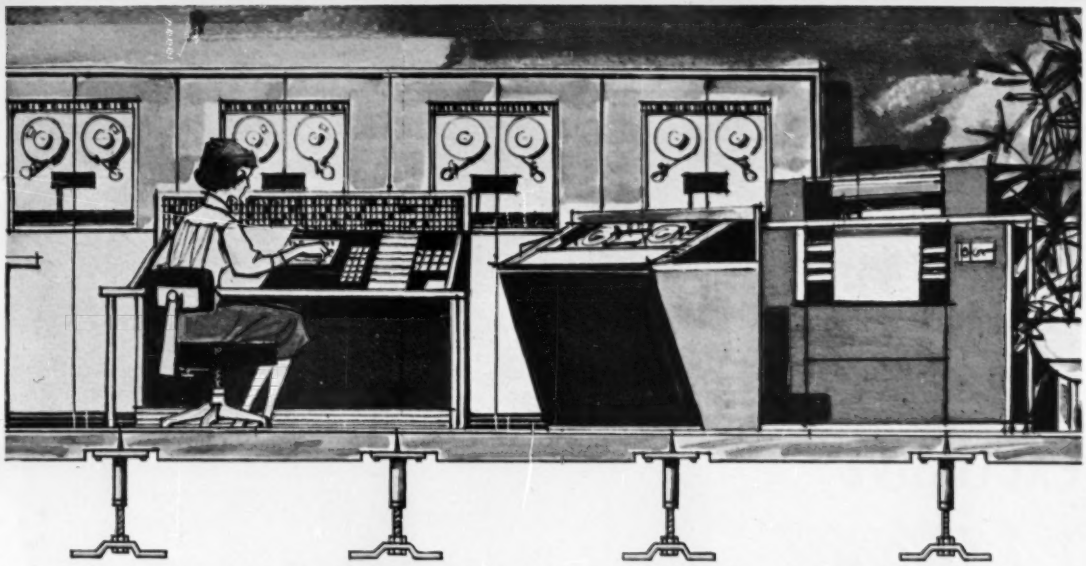

Greater plan flexibility and greater under-floor space with

LUPTON ALUMINUM RAISED FLOORING SYSTEM

For Electronic Data Processing Rooms

Designed specifically for computer installations, LUPTON Aluminum Raised Flooring provides a stable, attractive floor with plenty of space underneath for cables, ducts and wiring. It offers you a number of important advantages.

Flexibility and accuracy. LUPTON aluminum raised flooring consists of strong, lightweight aluminum floor panels supported by adjustable steel pedestals. These panels . . . accurately made to close tolerances . . . are 100% interchangeable. You can make changes and additions to your plan and achieve tight fit. You also have complete re-use of your standard components with new materials.

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LUPTON offers you its aluminum raised flooring system on either a materials delivered basis, or as a complete installation. Either way, LUPTON furnishes an experienced field supervisor during installation.

Write today for a comprehensive brochure on LUPTON's distinctively improved raised flooring system.

Total access to under-floor space. With the LUPTON aluminum raised flooring system, you can efficiently "lay in" cables rather than "thread" them. Locate cable or duct entry panels anywhere on the floor area. Make cutouts on the site.

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FOR THE FIRST TIME
a random memory device can be effectively utilized for both random or sequential processing.

FOR THE FIRST TIME
it is possible to store, sort, update, and report—using a single, magnetic file.

FOR THE FIRST TIME
it is economical and practical to employ multiple random access units in one system.

FOR THE FIRST TIME
a random access memory can be removed and a new memory mounted in approximately 30 seconds.

The National 315 will cut costs in any EDP system . . . both small and large-scale. National has taken a reel of magnetic tape—and in effect converted it into a deck of magnetic cards. Each deck of cards contains more information than can be stored in over 69,000 punched cards. In a single, magnetic card file system, National has combined all the advantages of all types of external memories.

National CRAM (Card Random Access Memory) does more work for less money. Here's how! *Flexibility:* data can be quickly selected at random or sequentially . . . over 88,000,000 alpha-numeric characters. *Speed:* the data on each card—instantly available—can be transferred at the rate of 100,000 alpha-numeric characters a second. *Convenience and Economy:* each deck of 256 cards is housed in an easy-to-remove card file that can be changed in less time than it takes to change a reel of magnetic tape.

National's Exclusive Magnetic Card File is only one of the oustanding features of the National 315 System. Learn why the National 315 is today's most economical computer investment. Call your nearby National Representative. Or write: Data Processing Systems and Sales, Dayton 9, Ohio

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CIRCLE 10 ON READER CARD

1961 IMPORTANT DATES

• National Telemetering Conference will be held May 22-24 in Chicago, Illinois.

• A Symposium on Large Memory Techniques for Computing Systems will be held on May 23-25 in the Department of Interior Auditorium on C St., between 18th and 19th Streets, NW., Washington, D.C.

• TRANSAC Users Group No. 8 will be held in Hartford, Conn. in May.

• NMAA Annual Meeting will be held June 28-30. For information contact William F. Mauk, NMAA Administrative Headquarters, 170 W. Central Rd., Mt. Prospect, Ill.

• The G-15 Users Exchange Conference will be held August 10-12 at the Denver Hilton Hotel, Denver, Colorado.

• WESCON is scheduled for the Cow Palace in San Francisco, Calif., August 22-25. For information contact WESCON Business Manager, 1435 La Cienega Blvd., Los Angeles, Calif.

• The National Symposium on Space Electronics and Telemetry will be held in Albuquerque, N.M., September 6-8. For information contact Dr. B. L. Basore, 2405 Parsifal, N. E., Albuquerque, N.M.

• International Symposium on tne Transmission and Processing of Information will be held at the Mass. Institute of Technology, Cambridge, Mass. September 6-8. For information contact Peter Elias, RLE, MIT, Cambridge 39, Mass.

• The 1961 Annual Meeting of the Association for Computing Machinery will be held at the Statler Hotel, Los Angeles, on September 6-8. For information contact Benjamin Handy, Chairman Local Arrangements Committee, Litton Industries, Inc., 11728 W. Olympic Blvd., Los Angeles, Calif.

• The Third International Congress on Cybernetics is scheduled for Namur, Belgium, September 11-15. For information contact Secretariat of The International Association for Cybernetics, 13 rue Basse Marcelle, Namur, Belgium.

floating floors

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FOR CONTROL DATA CORPORATION 1604

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Major problems encountered in the Package Concept have been the air conditioning equipment and electrical panel. To answer these problems, our Research and Development Department has designed and developed a complete mechanical equipment room within a Package. The size of the unit is 33″ wide by 72″ long by 72″ high, mounted on 8″ casters and weighing only 1,200 lbs.

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1.00 **AIR CONDITIONING**

1.01 Cooling capacity of 64,000 BTU net (6 HP) at 75°F city water or 54,000 BTU at 85°F cooling tower water.

1.02 Two separate 3 HP compressors circuited so that if one fails, the other compressor will operate as a standby. (When equipment is used with a pressurized floor plenum design).

1.03 One electrostatic filter rated at 70% (N. B. S.)

1.04 One visible chart recorder giving temperature and humidity records, which can be either a part of the Package or located where desired.

1.05 Air capacity of 2,750 CFM.

1.06 Sound and thermal insulation.

1.07 One condenser water hook up for heat release and humidity circuit. (Service line from source and connection by others).

1.08 One drain connector for relief of condensate. (Line from unit to drain outlet and connection by others).

1.09 Built in controls to meet seasonal conditions or room requirements to operate the compressors as required.

1.10 Humidification and temperature controls.

1.11 Humidifying capacity of 20 lbs. of water per hour.

1.12 Adjustable air outlet converter located on bottom side of unit to allow floor plenum use.

1.13 Electrical connection on side of unit to activate complete circuit.

2.00 **ELECTRICAL PANEL**

2.01 Main breaker for the 1604 incorporated in the Package Unit. (Power line from main source to main breaker by others).

2.02 Extra breakers mounted on electrical panel if required.

3.00 **FLOATING FLOOR**

3.01 600 sq. ft. of Floating Floor. (Marbleized vinyl tile 18″ x 18″ x ⅛″ with plastic lip edge).

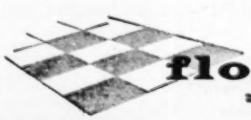
3.02 One ramp.

3.03 Fifteen cable cutouts.

3.04 20 lineal feet of air diffusers with dampers.

The above Package will handle approximately 600 sq. ft. based upon conditions, site location and condenser water temperature. Multiple units of the Package can be expanded as required.

floating floors TWX number is NY 1-3618



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CIRCLE 11 ON READER CARD

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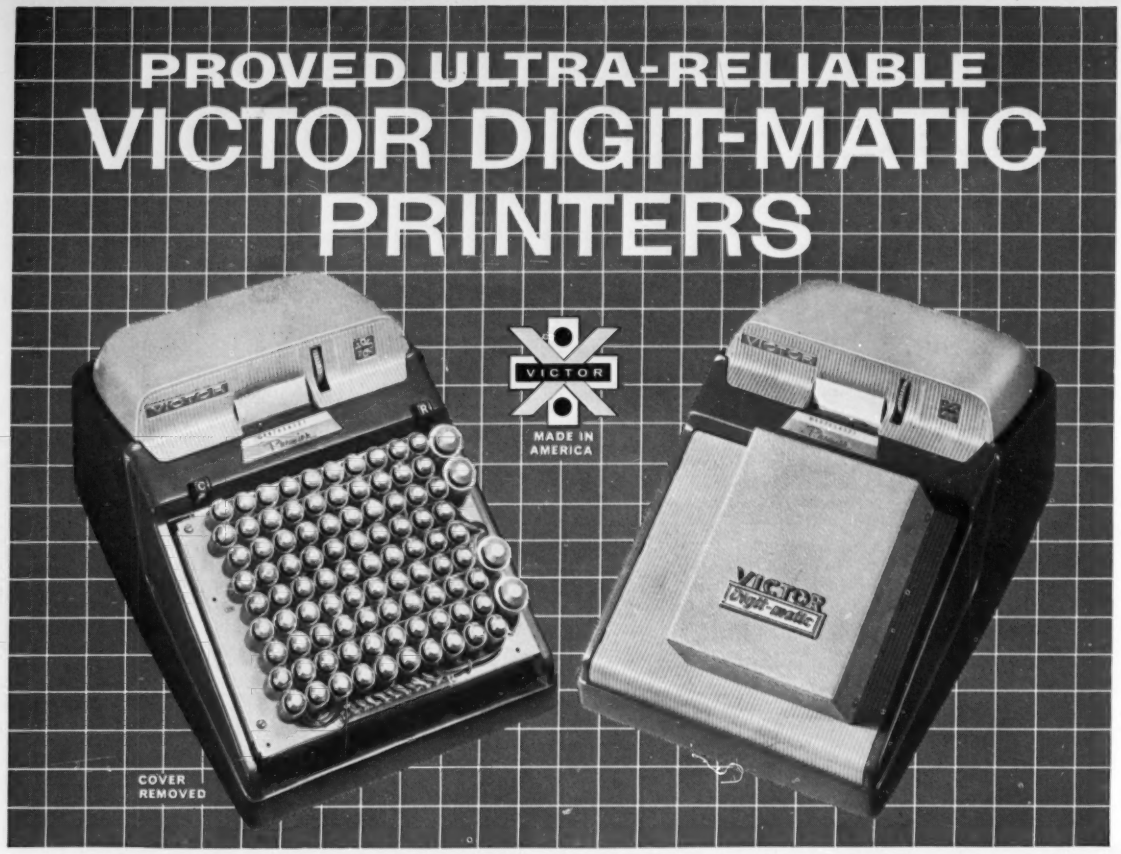

160,000,000 digit impressions without failure

Rugged, Trouble-Free—Digit-Matics are specially built to stand the strain of continuous operation. In a durability test, over 160 million digit impressions were made without breakdown or need of adjustment. The machine tested operated continuously, eight hours per day until 160 million digit impressions were made. During this period only normal lubrication and cleaning were performed.

Parallel or Serial Entry — Automatic and unattended, solenoid-activated Digit-Matics print out alpha-numeric data from remote equipment. High speed parallel entry models accept up to 10 digits at a time, print up to 4 lines per second. Serial entry models accept 1 digit at a time, up to 11 per line.

Two-Color Printing — Positive values in black, negative values in red. Ideal for "accept-reject" sequences, testing applications, accumulating data from two sources on one Digit-Matic, and many other uses.

Adaptable to Your Specific Needs — Line includes listers, accumulators and calculators. Versatile units can handle degrees, minutes, seconds, fractions. Other modifications: superimposed keyboard for manual use, time readings, counters, etc.

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CIRCLE 12 ON READER CARD

CDC 6600 IN STRETCH CLASS

From informed industry sources outside of Minneapolis' fast growing Control Data Corp., DATAMATION has learned of a major development in computer hardware and logical organization, which may be announced this Fall although basic design and specs are ready now. It's a STRETCH-class entry: CDC's 6600.

Although production and availability of the 6600 is over two years distant, it is strongly rumored that a letter of intent has been received from one of the larger AEC installations. The 6600 will lease from $150 - 200K per month.

While physically small by comparison to STRETCH-class hardware, the 6600 will feature a core storage of 256 K words; less than one microsecond considerably less than four, one microsecond add time, four microsecond multiply time and two multiplier units operating in parallel.

The 6600 will also feature a small amount of very fast registers, NOT CORE, from which instructions could be executed, and it will have the ability to use eight satellite computers to time-share the large memory. There is also the rumor of extremely fast tapes under development.

The 6600 has 8 peripheral processors with their own memory which are integral to the central computer. The entire system's performance will be 15 times faster than the 1604 and will have 20 megacycle circuitry throughout. It will have parallel processing ability with a "considerable amount" of parallelism in input/output.

The 6600 will be similar to the 1604 in that users will be able to hang boxes on it for use with competitive equipment.

Other important specs: it will have floating point capability with its 60 bit word divided into 48 bits for fractional use and 12 for exponent. Fixed point will be limited to 48 bits even though the word size is 60 bits.

Computing power for the 6600 will be derived from a unique logical design with multiphase memory.

First news of the computer was dropped by CDC President William Norris at a recent stockholders meeting. Although presented as a brief "off-the-record" remark by Norris, it was subsequently reported by local papers and the Wall Street Journal.

BIBBY TALKS TO UNIVAC USERS

RemRand President Dause L. Bibby flew out to Los Angeles last month to address the UNIVAC Users Assoc. Some quotable quotes follow . . . "The computer business has been picking up in spite of the recession because business is looking for ways to improve methods . . . We are spending 50% more this year on research . . . and are in the process of building up our field organization . . . I would be less than honest if I didn't admit that, with the exception of a few dogs we have and a few dogs the competition has, computers look strangely alike.

Here lie 707 rolls of paper tape shot full of holes by Tally Perforator #171

...Long may she run!

LIFE TESTING PROVES RELIABILITY OF TALLY READERS AND PUNCHES

The only way to really find out if a machine is reliable is to run it to death. That's what Tally engineers are literally doing with perforator #171 as part of a continuing program to prove and improve the accuracy and reliability of Tally tape equipment.

On October 20, 1960, perforator #171, chosen at random from a production run, started a life test with an alternate hole pattern verified by a Tally reader.

As of Feb. 13, 1961, perforator #171 had completed 70,700,000 cycles of accurate operation with only two minor mechanical break-downs. Repairs were made in a matter of minutes. This is a record of reliability that speaks for itself.

RELIABILITY IS ONE REASON TO CHOOSE TALLY

"State of the art" technical excellence is another. Only Tally punches give you the benefit of asynchronous operation. Speed is completely variable. A unique wire clutch lets you vary speed for slaving to other equipment which simplifies the design of logical systems.

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FOR A DEMONSTRATION OR MORE INFORMATION

You may arrange a demonstration or secure full technical information by calling your nearest field engineering office listed below or writing directly to factory.

P.S. *If you are having problems making complex multichannel programming tapes, call us about that too. We're making up 16 channel guaranteed error-free tapes for some of the nation's most sophisticated missile and satellite programs.*

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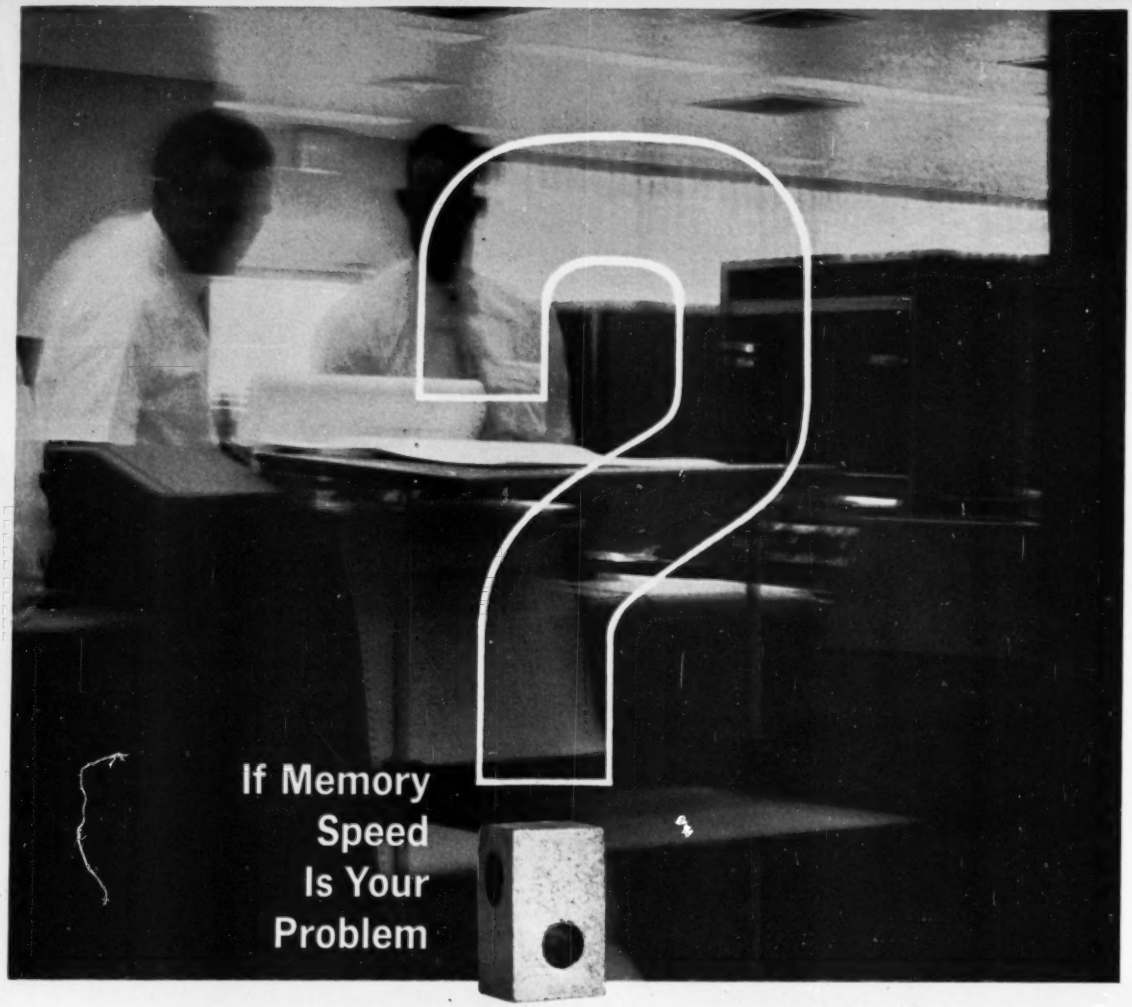
CIRCLE 14 ON READER CARD



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Specifications

Up to 1024 words
Up to 36 bits per word
Read cycle time: 1.0 μsecond
Access time: 0.4 μsecond
Loading: From paper tape or your equipment at rates up to 200 kc
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Temperature: 0°C to 50°C

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CIRCLE 15 ON READER CARD

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editor's readout

A NEW VOICE FOR COMPUTING

With the conclusion of the Western Joint Computer Conference on May 11th, the National Joint Computer Committee ceased to exist and sorrow for the deceased was in short supply.

Designed, chartered and functioning for the sole purpose of sponsoring joint computer conferences, NJCC was innately shackled to a noble but intrinsically limiting endeavor. Despite this fact, innumerable efforts were made to expand the Committee's sphere of accomplishment.

Invariably, when an ACM, IRE or AIEE member of the Committee offered a suggestion transcending computer conferences, he would be confronted with involved parliamentary debate and ultimately, the simple but firmly negative declaration, "We can't do that! . . . It's not in the charter!"

General dissatisfaction with the NJCC charter soon became a thorny factor in industry rapidly accelerating in a multitude of directions, many of which required opening new lines of communication with highly competent although laterally interested associations.

Last year, after much discussion, the late Harry Goode, then chairman of NJCC, called several informal and a number of not so informal meetings to see what could be done. The result: the origins of the American Federation of Information Processing Societies.

A constitution of AFIPS was submitted to the three member societies of NJCC and with considerably more than a modicum of enthusiasm has been unanimously ratified. On July 1st, AFIPS will be born.

The promise which AFIPS holds is that of a new, clear voice for the computing profession. Without infringing on the rights or activities of member societies, it will serve as a unifying force both on the national scene and internationally as the sponsor of the American representative to the International Federation of Information Processing Societies (IFIPS).

Specifically, AFIPS could and undoubtedly will sponsor computer oriented meetings with allied disciplines such as nuclear physics, chemical engineering, astro-physics, and others. Provision has been made in the AFIPS constitution for a widely expanding membership to encompass the broad perspective of business and scientific organizations.

The obvious need for an intelligently planned and carefully executed campaign of education and publicity can be filled by AFIPS. As a national voice for information processing, it is hoped that the public image of the profession will be swayed from "magic brains" and "composers of sausage recipes" to a more realistic concept of the contributions of computing.

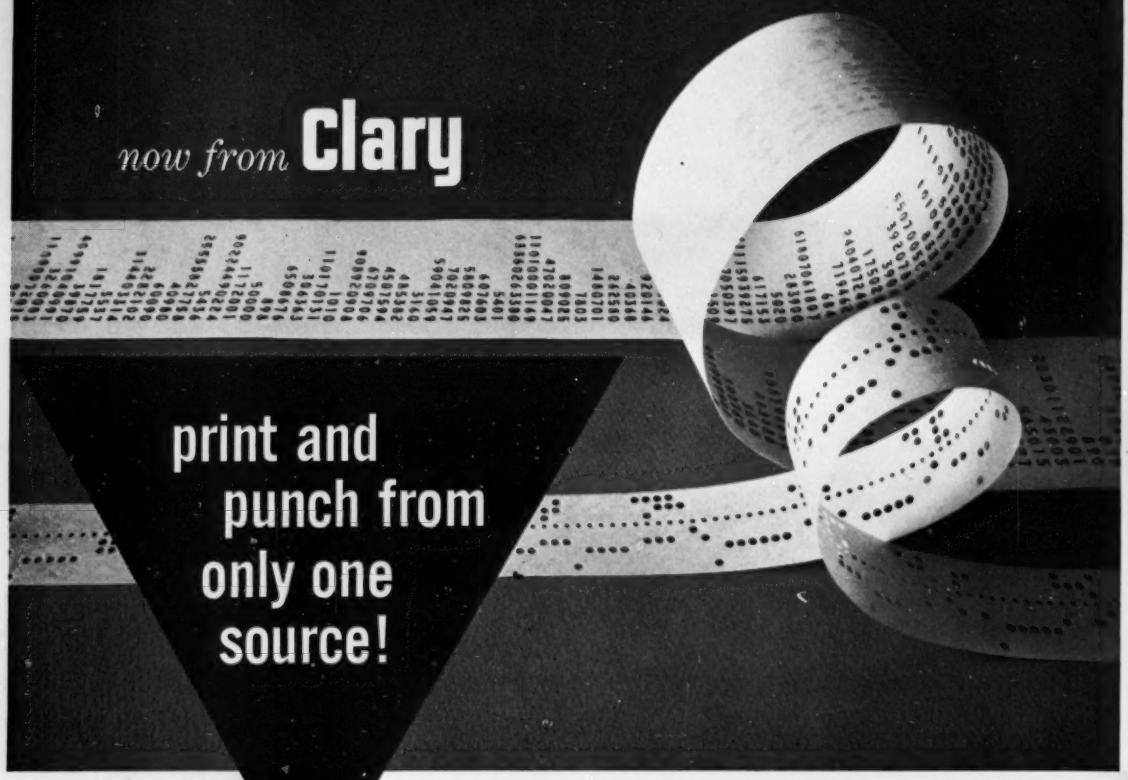
On the international scene, exchanges of concepts and personnel can prove an invaluable boon to the advancement of the profession and a major area for AFIPS participation. In such politically sensitive countries as the Soviet Union, a freer flow of information could be initiated and perpetuated only through the concerted efforts of an organization such as AFIPS via its participation in IFIPS.

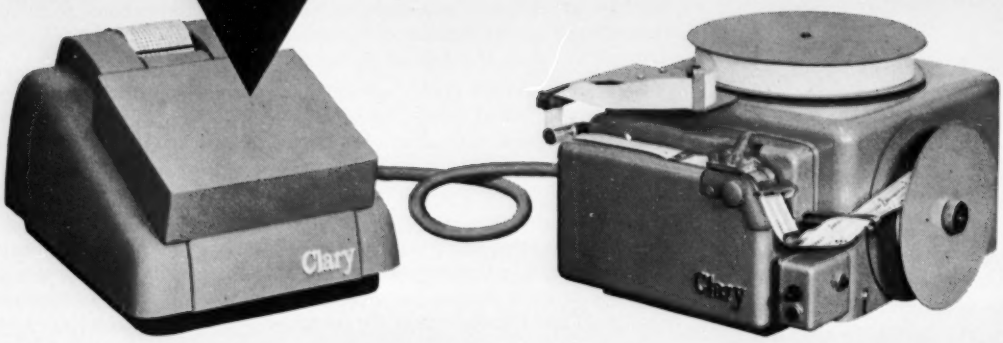
Because of the wide scope of these activities and the variety of influences which AFIPS must assimilate, it may be felt that restrictive covenants should be incorporated as unwritten procedure in AFIPS activity. This concern should be countered with a long evaluative look at the many unpalatable experiences with NJCC.

To properly focus its activities in a number of purposeful directions, AFIPS must retain the optimistic concept of its founders. Of prime importance at its inception is a forward-looking, nonregressive attitude tempered by good judgment but dominated by its larger function as an information processing society of societies.

now from **Clary**

print and punch from only one source!





Now, with just *one* output from the data source, you can record information in reusable form *two* different ways – on printed tape, and on punched tape.

The secret of this simpler, faster, more economical recording method is Clary's special printer-perforator combination. This versatile unit prints out information from a wide range of data sources and records it on a "common language" punched tape.

The taped data can be kept for permanent records... mailed or directly teletyped to distant points... used as language for computers, process control units, and in other industrial applications.

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The printer used may be serial or parallel entry. The tape perforator will punch any number up to 8 transversely-spaced code hole channels, and the format is programmable.

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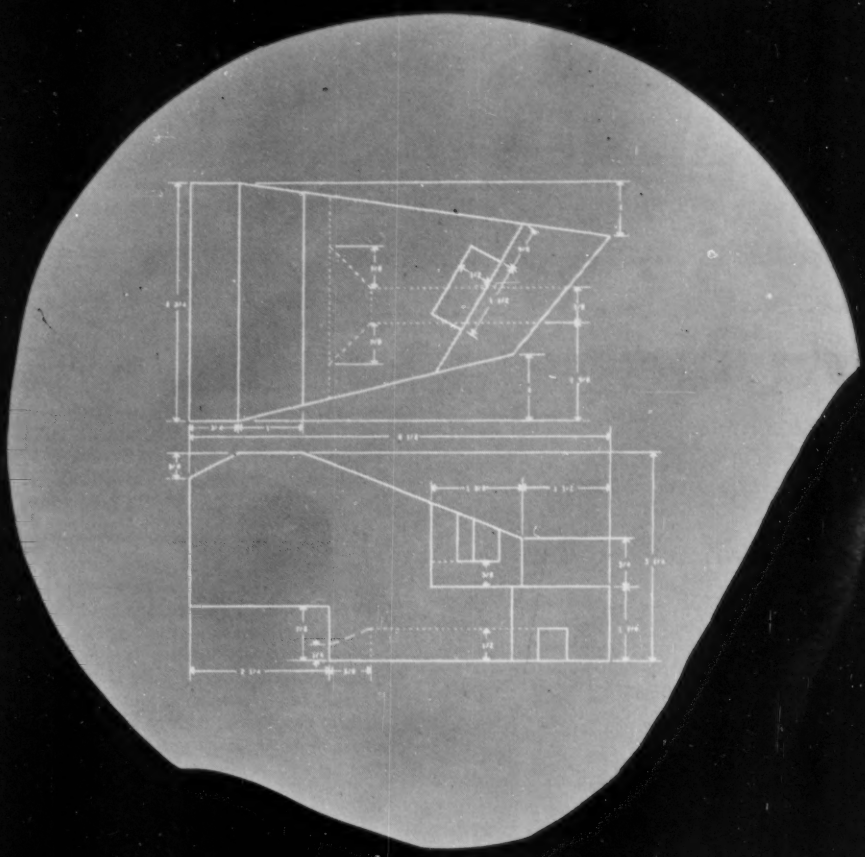

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GD

GENERAL DYNAMICS | ELECTRONICS

Emphasis on logic

DESIGN TRENDS FOR LARGE COMPUTER SYSTEMS

by CHARLES W. ADAMS,
Charles W. Adams Assoc., Bedford, Mass.

THE keynote in the design of new systems, whether large or small, is not hardware but logic. Consequently, new developments in physical hardware can be rather quickly summarized, with principal emphasis given to new approaches to internal logical operation.

new devices

The hardware development which caused so much excitement only a few years ago – solid-state circuitry, two-microsecond core storage cycles, magnetic tapes operating reliably at upwards of a hundred thousand characters per second, magnetic juke-boxes for "random" access to files of ten or twenty million characters, scanners for reading and interpreting printed numbers optically – are now taken for granted. Today the attention of the system designer is turned toward facilitating the effective utilization of these now almost human achievements in hardware design.

This is not to say that new developments are not being made in the hardware area. For one thing, rather spectacular improvements are being made in the reliability and costs associated with all aspects of computer componentry. Most notable perhaps are the continually improving performance of the large drums, disc files, optical scanners, and magnetic-ink character recognition devices (witness the new checks the banks are supplying to all their customers as part of the nation-wide adoption of MICR).

A new approach to random-access files has been announced by NCR, to wit the CRAM system involving automatically selected magnetizable sheets which are then wrapped around a drum. IBM demonstrated last year a "tractor" system for selecting tape reels automatically. The really new hardware seems, however, to be appearing primarily in the area of high-speed storage, both erasable and non-erasable.

non-erasable storage

Increased attention in being given to various forms of non-erasable (i.e., read-only) storage systems, large and small. Though new in detail, such devices are far from new in principle. Interest in them stems in part from increasing recognition of the potentialities of using "stored logic" in system design, and in part from the growing popularity of special-purpose stored program and/or stored data file systems.

One example of non-erasable storage is the 0.2-microsecond magnetic slug memory which will be used in the Ferranti Atlas computer to contain an executive routine for multi-programming control as well as such things as macro-program subroutines. Speed is the most important aspect of this device, but the fact that it can be altered only at the factory puts the Ferranti programmers in an enviable position indeed since no user can tamper with their programming package once it leaves the plant.

Various control computers use non-erasable memories such as drums with mechanically locked-out recording circuitry, twisters biased with permanent magnets, and non-destructive reading from thin-film storage. For example, Remington Rand announced some time ago a dual-film device in which an erasable cobalt film biases a read-only permalloy film, and is actually using Bell Labs twisters with magnets mounted on removable cards. In the M490 and 1206 they provide a small diode matrix, the contents of which can be mechanically altered only by inserting plugs pre-assembled with wires soldered in place, for use in loading error routines, etc. And, of course, more than ten years ago M.I.T.'s Whirlwind I was performing 125,000 instructions per second, working from a storage of 80 flip-flops and 432 diodes controlled by individual toggle switches.

A third class of non-erasable storage is photographic storage, optically scanned by cathode ray tubes, which yield a very large high bit-rate file – e.g., the IBM photoscopic disc memory for use in language translation and the BTL random-access photographic storage used in electronic telephone exchanges. In these cases, the emphasis is large volume data storage at reasonable costs and/or rather high speeds, while the fixed drums, twisters and diodes are aimed at protection against accidental loss of information (usually of a real-time control program).

high-speed storage devices

Reading or writing in a random-access storage in less than a microsecond is being accomplished in thin-film

magnetic memories on which the M.I.T. Lincoln Laboratory, Remington Rand, and Honeywell have announced some results. Small (128 words in the UNIVAC 1107 case) thin film storages operating at 0.6 microseconds are now functioning satisfactorily in the laboratory. A ten-thousand-word storage at 0.1 microseconds is the present objective at Lincoln Laboratory.

The National Cash Register Company has announced a magnetic rod memory storing a thousand bits per cubic inch with switching times of 0.05 microseconds.

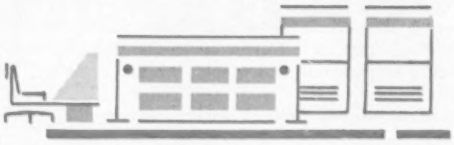
Aside from film and rod systems, work is apparently still continuing in the cryogenic area (involving superconductivity phenomena at temperatures near absolute zero), but no real breakthroughs have been made public.

increasing effective storage speed

Techniques for increasing the effective speed of a conventional magnetic core storage device include using two or more independent banks alternately, providing asynchronous operation in which rewriting is delayed if possible until storage access is not otherwise needed, and implementing look-ahead schemes by which any potentially idle time is used to read information in anticipation of its later use. The gain from such techniques is limited to a reasonably small percentage increase (under 100%) and certainly in practice has not always been as great as has been expected. In any event these are basically logical rather than physical means of increasing speed, akin to the various forms of autonomous operation discussed later.

new logical designs

The biggest design improvements in large digital computers during the next few years seems likely to come in the logical organization of the systems rather than in the componentry involved. The techniques employed and the objectives gained are many and various – so much so that what follows cannot lay claim to being even a comprehensive catalog, quite aside from not containing any appreciable degree of detail. What has been attempted, rather, is to make mention of a number of techniques and to assess their apparent purpose and merit.



arithmetic

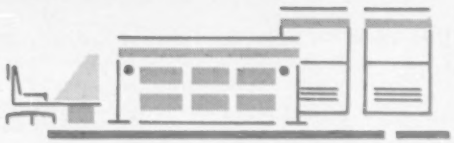
The age-old problem of choosing among binary, decimal, and alphanumerical operation has not been completely resolved, but the natural tendency is toward compromise: binary computers which have convenient facilities for conversion to decimal and even machines with two or more forms of operation built directly into the hardware (e.g., the Honeywell 800 and the RCA 601).

Effective storage capacity is sometimes increased by use of a short word length with built-in double-precision arithmetic to be used when needed without an excessive speed penalty (e.g., the Ramo-Wooldridge AN/UYK-1 and the Packard Bell 250). Alternatively, provision is made for dealing with half-words as in the Remington Rand 1107 and the IBM 7030.

Most large machines of course, have built-in floating point arithmetic at least as an optional feature, but the Bendix G20 is the only one being promoted as having no fixed point operations. (Provision is made for unnormalized floating operations which then are essentially fixed point). However, one sometimes encounters business men who will not consider the G20 because they definitely want to be able to do fixed point arithmetic.

address logic

Merely numbering storage locations consecutively from 0 to N is now old hat. Indirect addressing and "literals" permit instructions to operate on the contents of the location whose address is contained in "x" or, much more directly, on "x" itself. Both are convenient in certain cases, but designers who haven't bits to burn in their instruction words sometimes omit these features.



On the other end of the scale, when there are more storage registers than there are bits to distinguish between them in the instructions, bank addressing (Honeywell 800) or relative addressing (CDC 160) are sometimes used. The programmer often has little patience with these – to him they are merely a nuisance. But the obvious economy of storage they permit (since most instructions do, or can be made to, refer to nearby locations) has perhaps not been as widely recognized as it should.

Engineering problems occasionally deal with short numbers, but usually with fairly long ones, and never with very, very long ones. The business user, however, concerns himself with "fields", not variables, and his fields can and do run the gamut from a single bit (male or female?) to several hundred bits (home address). Character-addressable machines like the IBM 705 and RCA 501 (and many others) help dispose of this problem, but a more honest way of dealing with the situation appears to be "field addressing", as in the IBM 7070, in which the existence of words is admitted (the IBM 705 has of course a 5-character word length, but evidently is ashamed to mention it). Semantics aside, character addressability would be a very desirable feature if it could be accomplished in a parallel manner to preserve speed.

A novel addressing scheme is planned for the Ferranti Atlas computer. It is a "one-level store" in which a large drum logically comprises the main memory, each drum location being separately addressed, yet the programs actually operate from a large magnetic-core working storage. "Pages" of 512 words are "automatically" brought into core as needed, and copied back to the drum when the space is more urgently needed for another page. Every reference to storage requires that the page number be first processed against a list of all the pages already in core, and the appropriate core page used where possible. An executive routine in the "fixed store" (mentioned earlier) is used to decide which page to replace if the reference is to a page

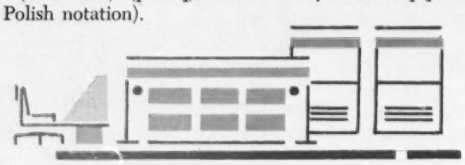
Mr. Adams' discussion of the state of the art in the area of logical design is representative of the outstanding material presented at the 1961 Western Joint Computer Conference held in Los Angeles earlier this month. Adams' unique Large Computer Systems Session was well received by conference attendees. In the June issue of DATAMATION, complete coverage of the WJCC sessions and exhibits will be accompanied by some interesting conference statistics. Outstanding papers and equipment will receive special mention and conference planners will assist in an evaluation of the 1961 meeting.

not already in core. The scanning of the list is done in a parallel fashion in a fraction of a microsecond.

instruction format and repertoire

Of the 35 commercially announced solid-state general purpose computers, 24 are single address and only the Honeywell 800 and 400 and the NCR 304 are three-address. The IBM 1401, 1410, and 1620, all the RCA systems, and the RW 400 are basically two-address machines but in a few cases four, three, two, one or no addresses are used in different operations.

More startling yet is the logic of the Burroughs B5000 which, they assert, "can well be considered the first non-vonNeumann computer." Operations are grouped into classes and the computer operates in arithmetic mode, subroutine mode, data-manipulation mode, or control mode, the last involving an executive routine permanently recorded on a magnetic drum. In arithmetic mode, the computer interprets a string of intermingled addresses and operations written in "Polish notation" (the expression $y = (w + i + t)\ (p - q)/z$ becomes $ywi + t + pq - xz =$ in Polish notation).



A number of interesting operation codes appear in some of the new computers, with the Remington Rand 1107 certainly among the leaders in the aspect of design. It is the stored-logic approach that holds the greatest fascination, however. The Ferranti Atlas, for example, uses one bit to make operation codes which are used as any built-in code but is executed by the computer as a subroutine stored in the fixed store. The Ramo-Wooldridge AN/UYK-1 on the other hand has no elaborate built-in operation at all and uses "lograms" of simple instructions to carry out more complex operations. Means are provided to go from logram to logram automatically, so that in use they behave much the same as conventional built-in instructions.

autonomous operation

To make effective use of each of the expensive high-performance magnetic tape units, core storage banks and arithmetic-logical elements in a large computer, each must be kept as busy as possible. Since different problems make different demands on the various units, proper balance can only be obtained by operating several programs at one time in the hope that the combination will provide a better distribution of demand. If a balanced load is to be thus achieved, each unit must be designed to operate autonomously, under its own control, and there must be an executive or scheduling procedure that keeps everything running as smoothly as possible.

The approaches to the control of a large system of autonomous units are several. In the IBM 7090, Bendix G20, and others, for example, elaborate input-output control units work out of the same storage as the central control, and means are usually provided to "trap" or interrupt the main program when the input-output control needs a new set of instructions. All of the scheduling is done by a part of the regularly stored program, although most users do not have to concern themselves with the question of this "driver" or "executive" routine.

The Honeywell 800 uses a highly-publicized multi-programming arrangement, in which each of up to eight different programs are performed virtually a step at a time in sequence. While a program is waiting for an input-output unit to function, it is by-passed with no idle computer time.

The Ferranti Atlas fixed store is used to hold an executive routine which is automatically called in whenever any autonomous unit needs attention and whenever the central computer is faced with any delay for input-output in the program currently being processed. Thus, the executive routine carries on moment-by-moment control of the scheduling, intermixing programs as required to give the best possible utilization of the system.

The Atlas also provides multiple consoles so that the separate programs may have separate operators. Furthermore, the executive routine can alter the page reference list (see above) according to what program is in use, so that the same "drum" location can be referred to by more than one program yet have no interference between them (the executive routine keeps track of the actual drum pages corresponding to the page numbers used in each program – the absolute addresses are in effect treated symbolically during operation).

The multiple consoles of the Atlas or the Bendix G20 make possible concurrent "on-line" program debugging by several programmers at one time. The Atlas scheme provides fool-proof protection of each program against accidental alteration by another sharing the machine at the same time. The potentialities and techniques of concurrent (autonomous) debugging would be a worthy subject for considerably more discussion than can be provided here.

modularity, graceful degradation

Intimately associated with the provision for and control of autonomous operations of control computers, storage banks, drums, tapes, in-out devices, consoles, etc., is the question of modularity and of providing for graceful degradation. This latter term is unfortunately not familiar to many computer designers – as will be seen, it refers to the behavior of the system in the face of malfunctioning of one or more of its parts.

Most present-day large computers are modular in that the user has a wide selection of usable configurations and correspondingly of system rental costs. In most cases, failure of a peripheral device affects only that part of the system, and the rest of the computer can continue in operation. But when any part of the central computer fails, the system is usually completely out of action.

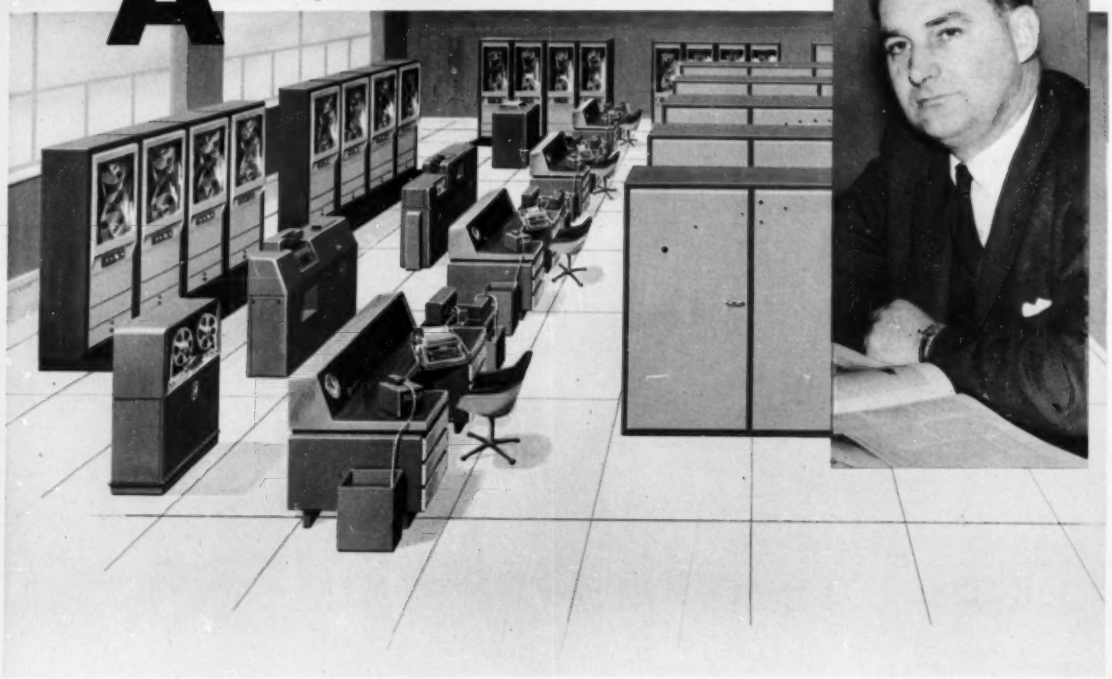
Graceful degradation is a design objective and for large systems is an important one. It implies that multiple central control units and storage banks are provided and are treated as autonomous units along with the tapes, etc. Using the philosophy of a telephone exchange, components are assigned to jobs as needed, and malfunctioning units are by-passed.

conclusion

It seems safe to predict that computer hardware will continue to gain in speed and particularly in reliability as the years go on. Almost equally certain is a continued trend toward stored logic and toward more autonomous operation in a multiprogrammed modular computer capable of some degree of graceful degradation. The results in terms of improved performance per dollar should be impressive.

NEXT MONTH IN DATAMATION

"Computer Simulation of Human Thinking and Problem Solving" by Newell & Simon will be a major feature in the June issue. Star billing will also be given to JOVIAL, System Development Corporation-designed language for writing computer programs in procedural statements. Post WJCC coverage, an insight into the merger of two important companies, a look at Europe's largest computer manufacturer and a detailed guide to what's IN and what's OUT in computing circles . . . these, and all our departments are on tap.



An artist's impression of a typical Atlas Computer installation.

Peter D. Hall, Manager of the Computer Department, Ferranti Limited.

Ferranti's heavyweight contender

THE ATLAS COMPUTER

by C. H. DEVONALD and
J. A. FOTHERINGHAM, Ferranti Ltd.

Co-operation between Ferranti Limited and Manchester University on computer design started in 1949 and was responsible for one of the early commercially available stored program computers. The latest machine to be designed jointly by Ferranti Limited and Manchester University is the Atlas Computer, which is representative of the "new generation" of computers; that is to say, large expandable internal memories, operation times of the order of one microsecond, and a design exhibiting features to provide efficient time sharing and parallel processing.

One of the most interesting features of Atlas is a "housekeeping" program, which is responsible for loading the system and allocating priorities with the object of achieving the best use of all equipment involved. The greater part of this program is stored permanently in a special fast access, read only, memory. This program also produces bookkeeping records, so that it can provide a detailed account of how much of the system each program is using. A basic Atlas installation will have several operating consoles, including one for site engineers, one for the main operator, and one for program check-out; and through each of these, the system can be used as though it were wholly devoted to the one job concerned.

the fixed store

In addition to the main immediate access store of ferrite cores, Atlas has also several thousand words of an entirely novel type of storage, to which access is extremely fast (.3 microseconds). The store consists of a wire mesh with small ferrite plugs inserted in the spaces, the contents of the store being determined by the presence or absence of a plug in each space. The store is fixed to the extent that it cannot be changed by program; to change it requires the physical insertion or removal of the plugs. It is envisaged that the store will be considered as part of the hardware of the machine, and not changed to any great extent after installation.

The existence of this type of storage has had two fundamental effects on the design of Atlas:

1. The more complicated functions required of the arithmetic unit will be performed by "subroutines" in the fixed store, though to the user they appear as individual functions of the order code. This means that it has been possible to keep the basic circuitry in the arithmetic unit simple, making it extremely fast, and yet to provide the computer with an unprecedented range of functions. For example, a large range of division functions, analytical functions (such as logarithm, expotential, sine and cosine), complex functions, double length floating point operations, vector operations, mixed radix conversion, and polynomial

evaluation, all appear as single functions in the order code.

2. Important organizational work can be performed by routines kept permanently in this fast store instead of by complicated and expensive circuitry. For instance, most peripheral equipments communicate with the central computer by means of fixed store programs, and as a result a wide variety of input and output mechanisms can be attached and used efficiently; further, the problems of attaching new peripheral equipment are considerably simplified.

A special additional section of core store is provided for use by the organizational program; thus core store, though similar in form to the programmer's store, is not part of it and is fully protected from interference by any "object" program.

overlapping operations

ATLAS is fully asynchronous, and as much overlapping of operations as possible is done. The core store is divided into "stacks" of 4096 words, each with independent access to the computing unit; these stacks are interleaved in pairs, even addressed words in one stack, odd words in the other, so that access to consecutive words of the store is not limited by the core cycle time. Instructions are drawn from the store in pairs, and the arithmetic unit is so arranged that while one operation is in progress, subsequent operations involving other parts of the computing unit can be proceeding at the same time. For example, while a full length multiplication operation is going on in the accumulator three or four indexing instructions can be completed.

Accesses to the store and to the various parts of the arithmetic unit are, of course, arranged so that an instruction dependent on the result of a previous operation will wait for the instruction to be completed (though the computer may go on to execute further instructions as well).

indexing and modification

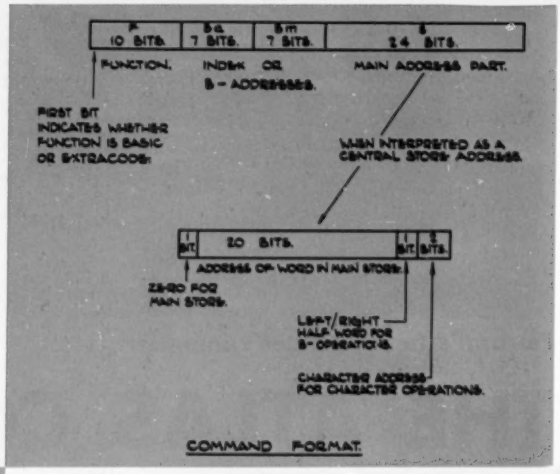
ATLAS has 128 index registers, numbered 0 through 127, of which 0 through 90 are available to the programmer for use in the normal way. The remaining index registers have various special functions. For example, index register 127 is the main control register, and unconditional jump is done by setting a number in this register. (Index register zero does not strictly exist, it is a dummy which always contains zero).

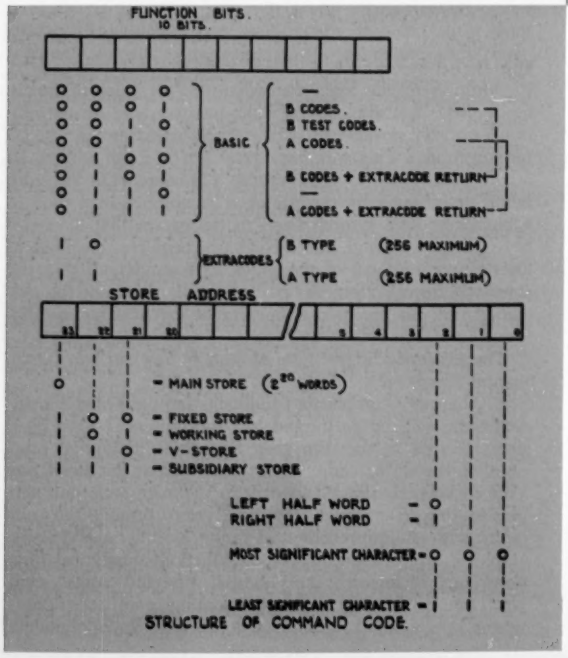
In an ATLAS instruction fourteen bits are allotted for the specifying of two index registers. In the case of accumulator instructions, the contents of both index registers are added to the address written in the instructions, giving double modification. In the case of indexing instructions, one index register contains the operand and the other is used as a modifier, providing (single) modification of indexing instructions.

The large number of index registers, and double modification of accumulator operations, are a great help in writing programs for ATLAS. In particular, compilers can take advantage of these features to produce efficient programs.

autonomous drum and magnetic tape transfers

Transfers of information to and from drums and magnetic tape units are direct to the core store, in units of 512 words, and once a transfer has been initiated it proceeds autonomously, leaving the computer free for other operations, and the magnetic tape decks are connected through eight channels, up to four decks per channel, so that eight tape transfers (each of which can be a read or a write) can take place in parallel.





time-sharing and parallel programming

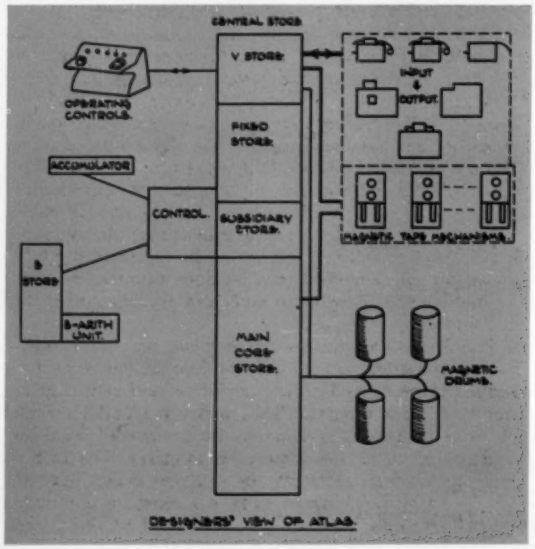
ATLAS possesses one of the most sophisticated time-sharing systems in existence today. All peripheral equipments are fully time-shared, and several programs can run independently in the computer at the same time. Such fully integrated time-sharing between programs makes it possible to make the maximum use of both the central computer and the peripheral devices. While one program has its operation held up because it is waiting for the operation of a peripheral device, work can be continuing on another program in the machine at the same time; also operations which would otherwise have to be performed off-line, on additional equipment, can be done through the central computer even though the computer is doing other work at the time.

The fixed store routines handling the peripherals operate on a time-sharing basis, taking the brief action necessary as and when required by the peripherals and returning control to a main program. This, and the parallel operation of main programs, is handled by an overall fixed store routine known as the Supervisor Program. The fact that this can be done efficiently by program makes it possible for the Supervisor Program to keep a record of the usage of the whole installation, and continually adjust the priorities of the various tasks to make the most efficient use of all the

Professor Tom Kilburn (right), Head of the Manchester University Computer Section, and assistant M. Lanigan.

equipment, including the central computer. As the requirements will be frequently altering as peripherals come in and out of operation and programs finish and new programs start, this continual re-assessment of priorities would be a prohibitive task for a human operator. The Supervisor Program also does the bookkeeping for the installation, using its knowledge of how much of the system each program uses.

Full lock-outs are built into the hardware, the Supervisor Program making it absolutely impossible for one program to refer unintentionally to a part of the machine or a peripheral device allotted to another program. Each program can make use of all index registers; when the Supervisor Program has to "suspend" a program, the contents of the index registers are preserved, and when the program is next able to continue, these settings of the index registers are restored. In this way it is made possible for programs to be written without any consideration of what other work may be put on the computer at the same time. Development of partially tested programs can be safely done on the machine while important standard programs



are running because there is full protection against a mistake in the untested program interfering with the operation of the others.

one-level store concept

The main store of ATLAS embodies a revolutionary system which enables the user to take full advantage of the whole main store, part cores and part drums, as though it was immediate access throughout. The facilities of a one level store are obtained though a major part of it may consist physically of drum storage. Information is grouped into units of 512 words, known as blocks, and it is these which are addressed by the programs in the machine.

The block addresses do not necessarily correspond to the physical positions of the blocks within the store. Associated with each block of the core store is a short register which holds the "address" of that block, that is to say the number that block is to be deemed to have. These registers are set, and on various occasions re-set, by the Supervisor Program. The locating of a block in the core store is done by a comparison, in parallel, between the required block number and the contents of the address registers. This comparison is extremely fast, and the time taken is included in the quoted times of instructions.

If a block is on the drum when it is required, a drum transfer is executed under the control of the Supervisor. The Supervisor decides which block at present in the core store should go to the drum to make way for the new block; it does this by means of a learning program which keeps account of the references to the blocks in the core store and determines which is least in use at the time. When the Supervisor brings a block to the cores, it also sets the block number in the appropriate address register.

With this concept the full advantages of sharing between programs can be realized. Each program can be written independently, and the amount of immediate access storage in use by each program at any instant is arranged by the Supervisor to give the maximum efficiency of use of the computer. Without the "one-level" store arrangement each program would have to be allotted its own fixed part of the core store. This would create a considerable problem of scheduling programs to share the machine, together with the difficulty of allotting to a program enough core store to make it efficient but not so much as to give it an undue share of the central computer. With ATLAS these problems disappear, and use of the store at any instant is determined by the whole configuration of the current demand

ATLAS SPECIFICATIONS

GENERAL CHARACTERISTICS

Mode of Operation	:	Binary, parallel, asynchronous.
Word Length	:	48 binary digits (= 8 characters of 6 bits each)
Data Representation	:	fixed point, floating point (octal exponent), 6 bit characters.
Accumulators	:	1 double length.
Index Registers	:	128
Instructions/Word	:	1
Instruction Format	:	

Function	Index	Index	Address (by characters)
10	7	7	24

STORAGE

Core Store:

Capacity (basic)	:	16,384 words
(maximum)	:	see below
Access time	:	0.75 microseconds

Drum Store:

Speed	:	5,000 r.p.m.
Size	:	24,576 words/drum
Capacity (basic)	:	4 drum = 98, 304 words
(maximum)	:	see below
Average access time	:	6 msec.*
Transfer time (512 words)	:	2 msec.*

*Computation and accesses to each drum can all proceed simultaneously.

The maximum capacity is 1,048,576 words divided between cores and drums as required.

Fixed Store:

Capacity (basic)	:	8,192 words
(maximum)	:	262,144 words
Access time	:	0.2 microseconds

OPERATIONAL SPEED

Addition, fixed or floating point	:	1.1 microsecond average
Multiplication, fixed or floating point	:	3.5 microsecond average

These figures include access to the operand from the core store. Average times have to be quoted because operations are overlapped for greater speed.

MAGNETIC TAPE

Characteristics	:	1" Ampex FR 300 A Tape.
Speed	:	90,000 6 bit characters/second.
Capacity	:	About 2,875,000 words to a 3,600 ft. reel of tape.

Maximum number of mechanisms: 32

Up to 8 tape transfers can be executed in parallel simultaneously with computing and drum transfers.

TIME SHARING

Interruption of the normal sequence of operation, caused either by peripheral equipment or by program, allows time sharing of all input and output operations and between several independent programs.

PERIPHERAL EQUIPMENT

Cards:	Input:	600 cards/minute
	Output:	100 cards/minute
Paper Tape: (5 or 7 hole)	Input:	300 and 1000 characters/second.
	Output:	60 and 300 characters/second.
Printers:		600 and 3000 lines/minute.

Other peripheral devices which can be attached include:

IBM Magnetic Tape (729 MK IV).
Flexowriters
Large Random Access Stores
Graphical Plotters
Data Links
Real Time Clocks
Etc.

on it, and not by the requirements of each program considered as a separate entity.

Drum transfers can also be executed under program control.

the monitor program

A part of the Supervisor routine is devoted to the reporting of errors in programs or data. When an error is detected, this part of the Supervisor is entered, and information about the cause of the error is printed out so that the fault can be pinpointed. In this way the machine itself can give considerable help in the checking out of programs; a valuable side effect is that all this information is in a written and therefore permanent form. Examples of faults causing entry to the Monitor section of the Supervisor are a meaningless code, a program grossly over-running its estimated time, a program referring to a block of information or a peripheral device not allotted to it, and some data being in the wrong format. During the monitoring of one program, the other programs of course proceed undisturbed.

the compiler of compilers

With ATLAS comes a new approach to symbolic programming. Dr. R. A. Brooker, of Manchester University, has devised a scheme going a level deeper than existing programming languages, a scheme in which any programming language can itself be defined. In effect, this scheme enables one to "teach" ATLAS any language one chooses, after which the computer can accept programs written in that language; it is a compiler of compilers. This greatly facilitates and speeds up the writing of compilers for ATLAS to accept programs written in other languages, including even the machine languages of other computers. The scheme has the big advantage that a compiler can be readily brought up to date as its language grows and develops.

internal checking

Every word in the core and drum stores carries an additional binary digit which is used as a parity check on the word. The parity is checked every time the word is referred to, and a failure causes entry to the monitor routine.

Each block on magnetic tape carries a check sum written at the end of the block. Information is recorded on the tape in stripes of 12 binary digits, and there are 2048 in a block. The check sum is two stripes, 24 digits, and consists of the sum of the 2048 12-bit stripes of information. On writing a block of information from the core store to magnetic tape, this check-sum is formed and written at the end of the block. While writing onto magnetic tape, a reading head immediately behind the writing head reads back the written information, and a second check-sum formed, which must agree with the check-sums formed as the information comes from the cores. Lastly, the check-sum written on the tape is also read back and must agree with the other two. If there is any disagreement the tape is moved back to the beginning of the block and the whole writing procedure is repeated.

After three successive failures to write correctly, the Supervisor enters a monitor routine to announce a write failure. On reading, the check-sum is reformed as the information comes off the tape, and it is checked against the one read from the tape. As on writing, a check failure causes a repeat of the operation and three successive failures cause an entry to the monitor.

progress on the Atlas project

A pilot model of the ATLAS System is currently running at the Ferranti Computing Factory in Manchester, England. This model has successfully proved the engineering techniques used in the project and is being used to train maintenance staff.

The first production machine is being delivered to Manchester University during the summer of this year and will be available for service work.

Underneath ELAFLOR'S aluminum or steel core panels, stands a *rigid grid system*, which provides unexcelled lateral strength at all floor heights. This system permits panels to be interchanged and cut-outs to be added or moved freely without the expense and trouble of releveling or extensive modification. Cable cut-outs, etc., can be made with complete flexibility . . . any size, any angle, any place . . . without decreasing load capacity or inducing side sway.

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CIRCLE 37 ON READER CARD

CIRCLE 114 ON READER CARD

Solid state
from Burroughs

design of the B 5000 SYSTEM

by WILLIAM LONERGAN and PAUL KING,
Product Planning, Data Processing Systems,
Burroughs Corporation

Computing systems have conventionally been designed via the 'hardware' route. Subsequent to design, these systems have been handed over to programming systems people for the development of a programming package to facilitate the use of the hardware. In contrast to this, the B 5000 system was designed from the start as a total hardware-software system. The assumption was made that higher level programming languages, such as ALGOL, should be used to the virtual exclusion of machine language programming, and that the system should largely be used to control its own operation. A hardware-free notation was utilized to design a processor with the desired word and symbol manipulative capabilities. Subsequently this model was translated into hardware specifications at which time cost constraints were considered.

design objectives

The fundamental design objective of the B 5000 system was the reduction of total problem through-put time. A second major objective was facilitation of changes both in programs and system configurations. Toward these objectives the following aspects of the total computer utilization problem were considered:

Statement of problems in higher-level machine-independent languages; efficiency of compilation of machine language; speed of compilation of machine language; program debugging in higher-level languages; problem set-up and load time; efficiency of system operation; ease of maintaining and making changes in existing programs, and ease of reprogramming when changes are made in a system configuration.

design criteria

Early in the design phase of the B 5000 system the following principles were established and adopted:

Program should be independent of its location and unmodified as stored at object time; data should be independent of its location; addressing of memory within a program should take advantage of contextual addressing schemes to reduce redundancy; provisions should be made for the generalized handling of indexing and subroutines; a full compliment of logical, relational and control operators should be provided to enable efficient translation of higher-level source languages such as ALGOL and COBOL; program syntax should permit an almost mechanical translation from source languages into efficient machine code; facilities should be provided to permit the system to largely control its own operation; input-output operations should be divorced from processing and should be handled by an operating system; multi-programming and true parallel processing (requires multiple processors) should be facilitated, and changes in system configuration (within certain broad limitations) should not require reprogramming.

system organization

The B 5000 system achieves its unique physical and operational modularity through the use of electronic switches which function logically like telephone crossbar switches. Figure 1 depicts the basic organization of the system as well as showing a maximum system.

master control program

A master control program will be provided with the B 5000 system. It will be stored on a portion of the magnetic drum. During normal operations, a small portion of the MCP will be contained in core memory. This portion will handle a large percentage of recurrent system operations. Other segments of the MCP will be called in from the magnetic drum, from time to time, as they are required to handle less frequently-occuring events, or system situations. Whenever the system is executing the master control program, it is said to be in the Control State. All entries to the Control State are made via 'interrupts.' A special operation is provided, which can only be executed when the system is in the Control State, to permit control to return to the object program it was executing at the time the 'interrupt' occurred.

The following are a few typical occurrences which causes an automatic 'interrupt' in the system: An input-output channel is available, an input-output operation has been completed or an indexing operation was attempted which violated the storage protection features built into the system.

In addition to processing interrupt conditions, the master control program handles fundamental parts of the total system operation such as the initiation of all input-output operations, tanking of input-output areas when required, file control, allocation of memory, scheduling of jobs (priority ratings, system requirements of each object program, and the present system configuration are considered), maintenance of an operations log and maintenance of a system description.

operating modes

The B 5000 can either operate with fixed-length words or with variable-length fields. These two modes of operation are called the word mode and the character mode. For certain operations, a processor operating on words is most desirable and for other operations, a variable field length mode of operation is most desirable. By combining both abilities in one processor, a processor can operate in the mode most desirable for the operation at hand. In a B 5000 system, it is even possible for one processor to be operating in the word mode and the other in the character mode.

When operating in the word mode, a standard format for the data word is used as illustrated in Figure 2.

Note that the standard word is an octal floating point word. However, the mantissa is treated as an integer rather

F—Flag (1 bit)
SE—Sign of Exponent (1 bit)
Exponent (6 bits)
SO—Sign of Operand (1 bit)
Integer Part (39 bits)

Figure 2
Data Word — Word Mode

than as a fraction (heretofore the reverse has been common practice). This provides two benefits: first, an integer has the same internal representation as its unnormalized floating point correspondent; and, second, the range of numbers that can be expressed, rather than being from 8^{+64} to 8^{-63}, is 8^{+76} to 8^{-51}. The first feature eliminates the need for fixed-to-floating point conversion; integers and floating point numbers can be mixed in arithmetic calculations. The second expands the range where trouble with range is most often encountered, namely, in numbers with extremely large magnitude.

The flag serves a dual purpose. The function of the flag depends on how the program references the data word. If the data word is a single variable and not an element of an array, the flag identifies the word as being operand, that is, a data word. If the word is an element of an array, the flag may be used to identify this particular element as an element of data which is not to be processed by the normal program. (for example, a boundary point in mesh calculations).

When operating in the character mode, each data word consists of eight alphanumeric characters as illustrated in

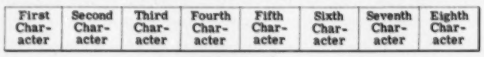


Figure 3
Data Word — Character Mode

Figure 3. Programs in the character mode can address any character in a word. Fields can start at any position in a word. A processor in a single operation can operate on fields of any length up to 63 characters long; operations on fields of greater length can easily be programmed. For example, two 57 character fields could be compared in a single operation.

There are two instances when the character mode operates with words of the type used in the word mode. Operations are provided in the character mode for converting numeric information in the alphanumeric representation to the standard word type of the word mode and vice versa. In both of these instances, the length of the alphanumeric fields being converted to or from the word mode type of word can be no greater than eight characters long. Again, conversion of fields of greater length can easily be programmed.

The purpose of the word mode is to provide the advantages of high-speed parallel operations, floating-point abilities and the inherent information density possible in a binary machine. In the first case, it is economically feasible to provide parallel operations in a word machine; the cost of parallel operations on variable length fields would be prohibitive. In the last case, a given size memory can contain over twenty percent more numeric information if that information is expressed in binary rather than binary-coded decimal, and over eighty percent more information than can be expressed in six-bit alphanumeric representation.

The purpose of the character mode is to provide editing, scanning, comparison and data manipulative abilities (although addition and subtraction are also provided). The type of editing facilities provided obviate the need for the artificial "add-shift-extract-store" type of editing. For example, operations are provided for generalized insertion of

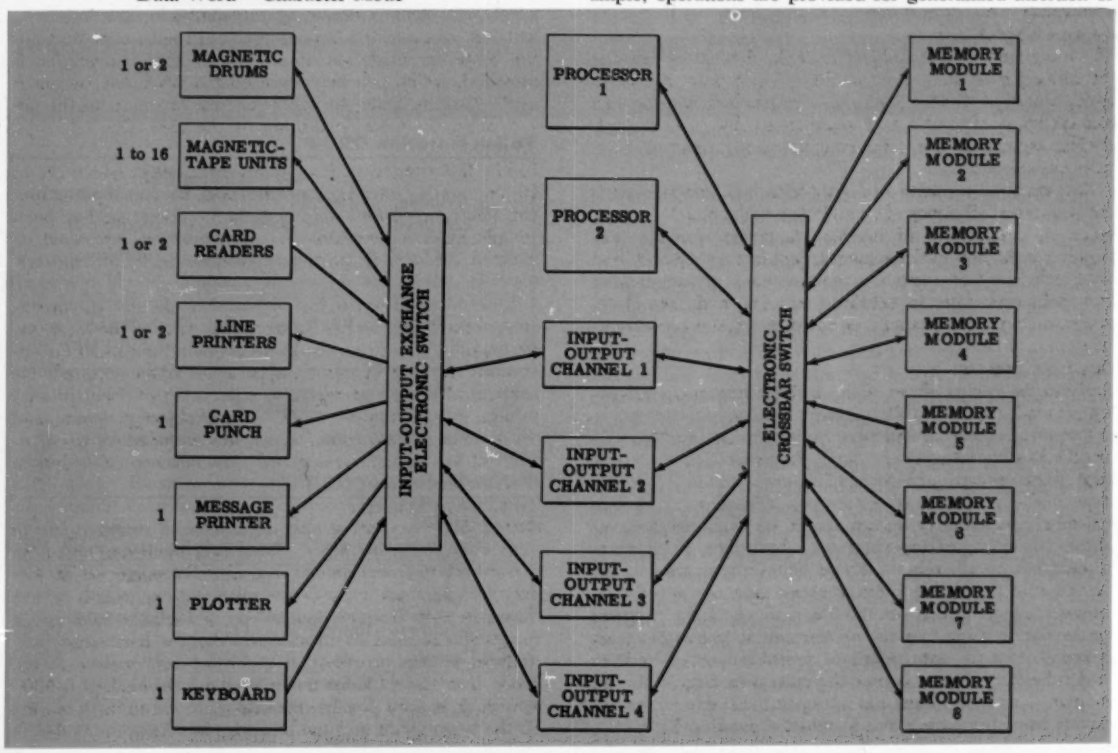


Figure 1
Organization of the B 5000 System

editing symbols (such as blanks, decimal points, floating dollar signs, etc.) and for the substitution or suppression of any unwanted characters. For those interested in the new area of Information Processing Languages, the character mode is particularly well suited to list structures.

program organization

Programs in the B 5000 are composed of strings of syllables. A syllable is the basic unit of the program and is twelve bits in length. The term "syllable" is used rather than instruction to distinguish it from conventional single-address or multi-address instructions. Each program word contains four syllables and they are executed sequentially in a left-to-right order within the program word, and sequentially by word. Branching is allowed to any syllable within a word. Before delving into some of the details of the internal operation of the B 5000 processor, it is necessary to discuss stacks, Polish notation, and the Program Reference Table.

the stack

The internal organization of single-address computers forces the wasting of both programming and running time for the storage and recall of the intermediate results in the sequence of computation. The data must be placed into the proper registers and memory cells before the operation can be executed, and their contents must often be completely rearranged before the next operation can be performed. Multi-address computers are constructed to make the execution of a few selected operations more efficient, but at the expense of building inefficiencies into all the rest. Automatic programming aids attack this problem indirectly: they relieve the programmer of the need to laboriously code his way around machine design, but they still must provide object coding to accomplish the storage and recall functions. In brief, conventionally designed computers, with or without automatic programming aids, require the wasteful expenditure of programming effort, memory capacity, and running time to overcome the limitations of their internal organization.

The problem is attacked directly in the B 5000 by incorporation of a "pushdown" stack, which completely eliminates the need for instructions (coded or compiled) to store or recall intermediate results.

In a B 5000 processor, the stack is composed of a pair of registers, the A and B registers, and a memory area. As operands are picked up by the programs, they are placed in the A register. If the A register already contains a word of information, that word is transferred to the B register prior to loading the operand into the A register. If the B register is also occupied by information, then the word in B is stored in a memory area defined by an address register S. Then the word in A can be transferred to B and the operand brought into the A register. The new word coming into the stack has pushed down the information previously held in the registers. As each pushdown occurs, the address in the S register is automatically increased by one. The information contained in the registers is the last information entered into the stack; the stack operates on a "last in - first out" principle. As information is operated on in the stack, operands are eliminated from the stack and results of operations are returned to the stack. As information in the stack is used up by operations being performed, it is possible to cause "pushups," i.e., a word is brought from the memory area addressed by the S register, and the address in the S register is decreased by one.

To eliminate unnecessary pushdowns and pushups, the A and B registers both have indicators used for remembering whether the registers contain information or are empty. When an operand is to be placed in the stack and either of the registers is empty, no pushdown into memory occurs. Also, when an operation leaves one or both of the registers empty, no automatic pushup occurs.

polish notation

The Polish logician, J. Lukasiewicz, developed a notation which allows the writing of algebraic or logical expressions which do not require grouping symbols and operator precedence conventions. For example, parentheses are necessary as grouping symbols in the expression A(B+C) to convey the desired interpretation of the expression. In the expression A+B/C, the normal interpretation is A+(B/C), rather than (A+B)/C, because of the convention that the / operator is of higher precedence than the + operator. The right-hand Polish notation used in the B 5000 is based on placing the operators to the right of their operands: A + B becomes AB+ in Polish notation. A+B+C can be written either as AB+C+, or as ABC++. In the expression ABC++, the first + operator says to add the operands B and C. The second + operator says to add A to the sum of B and C. Returning to the first examples above, A(B+C) can be written as BC+A× or ABC+× in Polish. The second example is written as BC/A+ or ABC/+. The extension of Polish notation to handle equations is shown in the following example:

Conventional notation Z=A(B - C)/(D+E)
Polish notation ABC - ×DE+/Z=

the stack in use

To illustrate the functioning of the stack, two simple examples are shown in Figures 4 and 5. In the examples, the letters P, Q and R represent syllables in the program that cause the operands P, Q, and R to be picked up and placed in the stack. The symbols + and × represent syllables that cause the add and multiply operations to occur. The two examples represent different ways of writing P(Q+R) in Polish notation. The first example in Figure 4 does not require pushdowns or pushups. The second example, shown in Figure 5, requires a pushdown in the execution of the syllable R, and a pushup in the execution of the syllable ×. The columns in the table represent the contents of the various registers after execution of the syllable listed in the first column.

Polish Notation QR+P×

Syllable Executed	Contents of Register A	Contents of Register B
Q	Q	Empty
R	R	Q
+	Empty	R+Q
P	P	R+Q
×	Empty	P(R+Q)

Figure 4

Polish Notation PQR+×

Syllabel Executed		Register A	Register B	Register S	Cell 101
P		P	Empty	100	–
Q		Q	P	100	–
R	Pushdown	Empty	Q	101	P
	Execute	R	Q	101	P
+		Empty	Q–R	101	P
×	Pushup	Q–R	P	100	–
	Execute	Empty	P(Q–R)	100	–

Figure 5

Ray R. Eppert, Burroughs Corporation president, points out the "modular" construction of the company's new solid state B 5000 system. With Eppert are James R. Bradburn, vice president – manufacturing and engineering, left, and Ken T. Hement, vice president – marketing.

independence of addressing

One of the goals set in the design of the B 5000 was to make the programs independent of the actual memory locations of both the program itself and the data, in order to provide really automatic program segmentation. Through automatic program segmentation, it is possible to have program size practically independent of the size of core memory. The systems analyst or programmer intending to do multi-processing is then no longer faced with the difficult task of planning what jobs are to be run together in order that system storage capacities are not exceeded.

In achieving independence of addressing, a solution requiring large contiguous areas of memory was not deemed satisfactory. Each segment of the program and each data area should be completely relocatable without modification to the program. It is then possible to load all the segments of a program or programs onto the drum at load time and call in the segments to any available space in core memory as needed during run time. If some segment of a program is overlaid by a subsequent segment of a program, the segment of the program destroyed in core memory is still available on the drum to be called in again if needed.

Due to the very high program densities in the B 5000, the availability of high capacity drum storage on every system and automatic segmentation, a minimum B 5000 system has the capacity for a program or programs equivalent to approximately 40,000 to 60,000 single address instructions. Of course, if an installation normally ran such large programs, the system would very likely not be a minimum system. However, the installation having an occasional need to run very large programs is not prevented from doing so by storage capacity.

Processing speed now becomes a function of the size of core memory. If large programs are run in a system with small core memory, time will be consumed in recalling program segments from drum to core. If the core memory is expanded, less time will be spent in such activity and the program or programs will be speeded up, and no reprogramming is required.

program reference table

The means of achieving independence of addressing in the B 5000 is called a Program Reference Table (PRT). The PRT is a 1,025 word relocatable area in memory used primarily for storing control words that locate data areas or program segments. There are also control words for describing input-output operations. These control words, called descriptors, contain the base address and size of data areas, program segments and input-output areas. A descriptor specifying an input-output operation also contains the designation of the unit to be used and the type of operation to be performed. Operands may also be stored in the PRT, providing direct access to single values such as indices, counts, control totals, etc.

In the word mode of the B 5000, every item of data is considered to be either a single value or an element of an array of data. If it is a single value, it will be obtained directly by indexing a descriptor contained in the PRT.

Program segments are described by program descrip-

tors. In addition to core base address, the program descriptor contains the location in drum storage of the program segment and an indication if the program segment is currently in core memory starting at the address specified in the descriptor. Entry to a program segment is made via its program descriptor contained in the PRT. If the program segment is in core memory, entry will be made to the program segment. However, when entry is attempted to a program segment whose descriptor indicates that the segment is not in core memory, automatic entry to the Master Control Program will occur and the desired segment will then be brought in from the drum. Notice that in moving from one segment to another, it is not necessary to know whether the segment to be entered is currently in core memory. Branching within a program segment is self-relative, i.e., the distance to jump either forward or backward is specified, not the address to be jumped to.

As a result of keeping all actual addresses of data and program in the PRT, the program itself does not contain any addresses, but only references to the PRT. To specify one of the 1,024 positions in the PRT requires only 10 bits which contributes greatly to the high program density achieved in the B 5000. Since the PRT is relocatable, references to the PRT contained in the program are to relative locations, thus completely freeing the program from any dependence whatsoever on actual memory locations.

word mode program

The word mode of the B 5000 processor has four types of syllables. The syllable type is distinguished by the two high-order bits of each 12-bit syllable. The types of syllable and the identification bits are:

00 – Operator Syllable
01 – Literal Syllable
10 – Operand Call Syllable
11 – Descriptor Call Syllable

The first of these, the operator syllable, causes operations to be performed. The remaining ten bits of the operator syllable are the operation codes. There are approximately sixty different operations in the word mode. For those operations requiring an operand or operands, the processor checks for sufficient operands in the registers; if they are not there, pushups from the stack in memory occur automatically.

The literal syllable is used for placing constants in the stack to be used as operands. The ten bits of the literal syllable are transferred to the stack. This allows the program to contain integers less than 1024 as constants.

The operand call syllable, and the descriptor call syllable address locations in the program reference table. The purpose of the operand call syllable is to place an operand in the stack; the purpose of the descriptor call syllable is to place the address of an operand, a descriptor, in the stack. There are four situations that arise, depending on the word read from the program reference table.

1. The word is an operand.
2. The word is a descriptor containing the address of the operand.
3. The word is a descriptor containing the base address of the data area in which the operand resides.
4. The word is a program descriptor containing the base address of a subroutine.

For (1), the operand call syllable has completed its action by placing an operand in the stack. The descriptor call syllable will cause the construction of a descriptor of the operand, replacing the operand by the constructed descriptor.

For (2), the operand call syllable then reads the operand from the cell addressed. The descriptor call syllable has completed its action.

For (3), indexing of the descriptor by the item that is now the second item in the stack occurs. For an operand call syllable, the operand is obtained from the indexed address; for the descriptor call syllable, action is complete after the indexing.

In the case of (4), subroutine entry occurs to the subroutine addressed. A word of the three previous types may be left in the registers upon return from the subroutine, in which instance the actions described above will take place, depending upon the type of syllable which initiated the subroutine.

Essentially, the four types of action that occur for an operand call syllable are obtaining an operand directly, indirectly, from an array, or by computation. Sometimes in the use of the call syllables, it is not known which type of action will occur for a particular syllable when the program is created. This is particularly true for call syllables in subroutines.

Programs in the word mode consist of strings of syllables which follow the rules of Polish notation. Variable length strings of call syllables and literal syllables, which place items of information in the stack, are followed by operator syllables which perform their operations on information in the stack.

The indexing features of the B 5000 allow generalized indexing and at the same time provide complete storage protection. Data areas and program segments of different programs may be intermingled, but a program is prevented from storing outside of its data areas. The method of indexing allows any of the 1,024 words of the program reference table to be considered index registers. Multilevel indexing is provided, i.e., indices of arrays can themselves be elements of arrays.

The subroutine control provided in the B 5000 allows nesting of subroutines – even recursive nesting (a subroutine is a subroutine of itself) – arbitrarily deep. Dynamic allocation of storage for parameter lists and temporary working storage simplify the use of subroutines. Storage is automatically allocated and deallocated as required.

character mode program

In the character mode of the B 5000 Processor, there is only one type of syllable, called the operator syllable. Program segments in the character mode are constructed of strings of these syllables. The character mode is designed to provide editing, formatting, comparison, and other forms of data manipulation. In doing so, the processor uses two areas of memory – the source and destination areas. When a program switches from word mode to character mode, two descriptors containing the base addresses of these areas are supplied. The source area or destination area may be changed at any time during character mode so that the program may act on several areas.

The character mode operator syllable is split into two 6-bit parts; the last part specifies the operation to be performed and the first part specifies the number of times the operation is to be performed. Operations are provided for the transferring, deletion, comparison, and insertion of characters or bits. Also, there are operations which allow the repetition of syllable strings. This is quite useful for complex table look-up operations and for editing information which contains repeated patterns.

conclusion

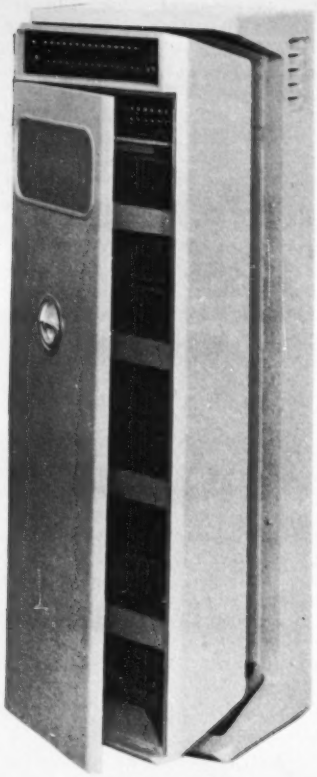
The Burroughs B 5000 system has been designed as an integrated hardware-software package which offers such benefits as savings in the memory space required to store equivalent object programs; multi-processing and parallel processing; and running, identical programs on systems with different size memories and different system configrations with no loss in individual system efficiency.

CIRCLE 115 ON READER CARD

Ramo-Wooldridge's AN/UYK-1

A STORED LOGIC COMPUTER

By H. M. SEMARNE and R. E. PORTER, Programming Development Section, Information Systems Department, Ramo-Wooldridge.



The "practical user" of computers may be described as the man who wants computing machinery to assist him in his work, but who does not want that machinery to become an object of independent study. To this practical user, programming is likely to be a necessary task which he may perform with skill and alacrity, but without a desire to get involved in the development of programming science. If he requires only a small computing installation, he may not have the services of computing specialists who speak to a machine in its own language. The practical user, with his particular purpose in mind, may then need direct personal access to his computer. He would want this access to be both easy and natural. The various types of automatic coding systems which have been designed to meet such a user's needs have greatly diminished the pressure on him to become proficient in machine language.

interpretive systems

Interpretive systems have also, in general, minimized the user's mixed blessing of exerting himself in the programming and coding stages to make his programs efficient. Although efficiency may mean not just elegance but possibly significant savings to him, the design and adaptation of coding systems to individual purposes has remained beyond the practical user's reach. He is often obliged to give up hopes of casting a program in a form really suited to his work, and has to settle for a general-purpose system. The cost of this settlement is often said to be amply compensated for by the advantage of machine use without machine specialization. If accurate appraisals of drawbacks and advantages were obtainable, it would still appear that any net benefit to the user must depend on the nature of the system and of the machine, on the nature of the application, and on time and manpower available. One thing is certain: through the use of an interpretive system, the performance rate of a machine may be decreased by a factor of ten or fifteen, a factor due to having the machine painstakingly translate, instruction by instruction, the pseudo-code which the practical user writes more easily than the machine language. Such a drastic slow-down may trouble only the expert programmer, though it also degrades the efficiency of the machine for the practical user. Clearly, a concept offering "interpretation without deceleration" would be a gain for all.

The Stored Logic concept offers help in this direction.

the stored logic concept

One may consider computer instruction types as rungs on an "abstraction ladder" rising from machine language toward natural human language, with distance from the bottom denoting level of abstraction with respect to the computer logic. Since abstraction levels may vary among machines, a flexible rope ladder will serve for purposes of representation, and no attempt at calibration will be made. The rungs of the rope ladder indicate general **instruction types.**

The practical user, desiring to instruct his machine in his own natural language, descends only with great reluctance toward the lower ladder rungs. The expert programmer goes the remaining "distance" to communicate with the machine in **its language.**

The customary machine instructions are well up the abstraction ladder and, of course, interpretive macro-commands, each of which stands for a sequence of machine instructions, appear even higher on the ladder. The bottom rung of the instruction ladder is held by the primary building-blocks of all types of computer instruction, namely micro-commands which cause the machine to open gates, trigger flip-flops, and perform other useful circuit functions.

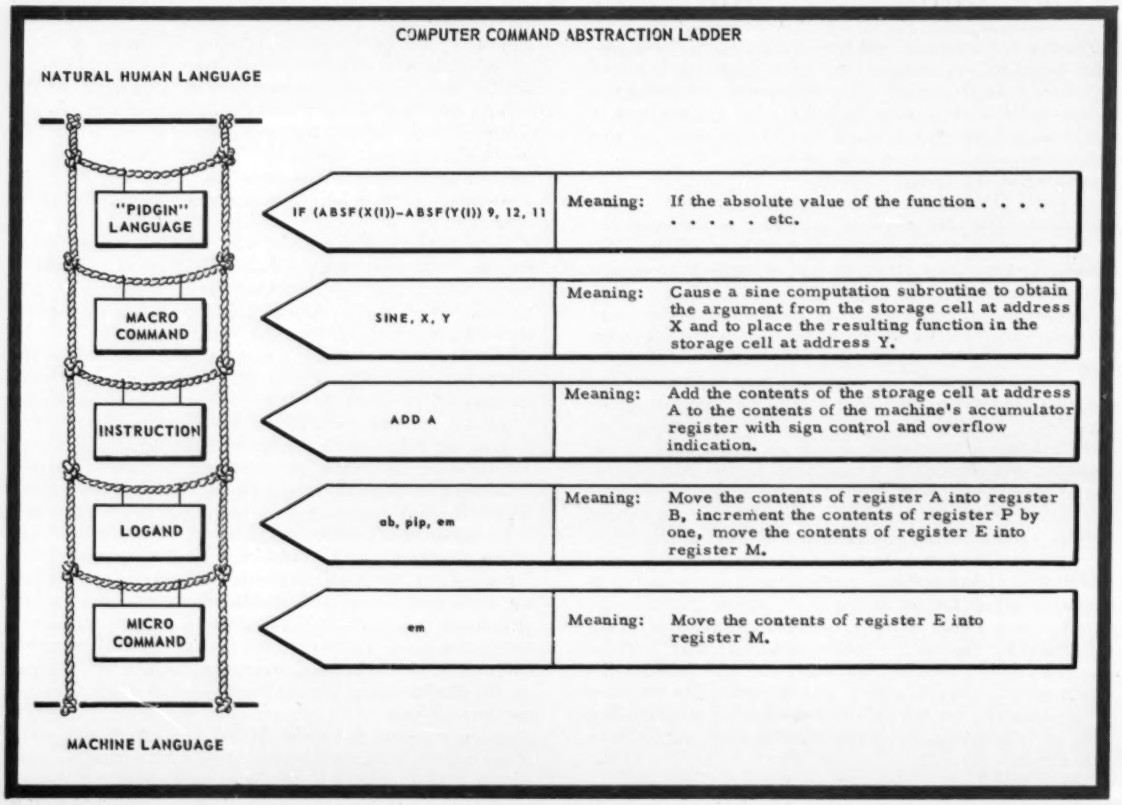
In the Stored Logic concept, much of the wired logic which mechanizes the machine-language instructions customarily found in an instruction list is disregarded, and only the basic logic expressed by the micro-commands is implemented by hardware. The logic for any instructions above the micro-command level is stored in the computer memory in the form of a micro-program, i.e., a sequence of micro-commands. Hence, in the Stored Logic concept, any type of instruction can be made up out of micro-commands and stored in memory access as a macro-instruction. Thus, conventional machine language differs from an interpretive system only by a degree of abstraction, i.e., by the

number of micro-commands required to form its instructions as compared with those of the interpreter. By replacing wired logic with sequences of micro-commands stored in memory, the Stored Logic concept allows the instantaneous logical organization of the computer to be specified as part of the program. Naturally, for the practical user, this precludes the need of an elaborate hardware package which would produce instructions no more – and often less – efficiently than a stored logic package. Furthermore, the stored logic package would be minimal, i.e., would include logic only for those instructions which the user requires in his work. A hardware package, of fixed construction for all uses and users of a machine, necessarily has logic for many instructions not required in a given application.

On the other hand, the user of a fixed-logic machine may strongly wish to have available as instructions certain useful composite operations which must be implemented by subroutines built up from machine instructions. Such subroutines, of course, belong above the interpretive level, high above that of machine instructions on the comparative graph of command types. Adaptability being the principal purpose of the Stored Logic concept, complex subroutines are dealt with as readily as an add-instruction. In each case, an appropriate chain of micro-commands provides all operations that one may wish to execute by one instruction. Consequently, the user is in a position to stock his machine with all those and only those instructions which he wants to use. Then, by a simple read-in, he can change the repertoire of the language of his machine completely. As an extreme application of the Stored Logic concept, one might visualize a stored logic machine simulating a given conventional machine and doing this with a decided advantage in speed, as well as in hardware cost. The real, and realistic, strength of the stored logic machine would, however, lie in its user-designed instruction list, not in its occasional ability to beat a fixed-logic machine at the performance of its own commands.

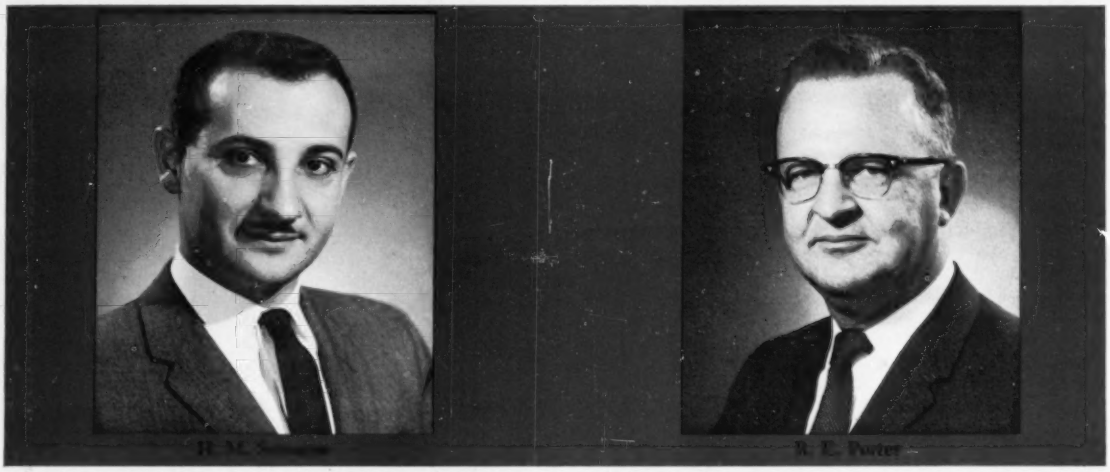
Repetitiousness in the sequencing of micro-commands may be tedious; excessive attention may have to be given to the checking-out of such sequences; and packing-unpacking procedures for micro-commands may be undesirable as solutions to a possible problem of excessive memory fill. Consequently, it is advisable at this time to adulterate somewhat the pristine rigor of micro-commands, with a gain in practical efficiency and without loss of principle within the Stored Logic concept. Micro-commands are combined, at the hardware stage, in clusters, each of which refines several operations, such as are frequently micro-coded in close sequence. These small clusters of micro-commands form elementary **logic commands** referred to as LOGANDS.

While logands can still be regarded as building-blocks of stored logic, their use has several advantages over that of their component micro-commands. Each logand will occupy a full word in memory; far less memory space and programmer attention will be demanded by a stored logic package composed of logand sequences than by one composed of micro-command sequences; and individual logands are more readily recognized as familiar instruction types than are micro-commands. Besides, in this clustering of micro-commands, the original freedom in forming such subsequences, just as required, will virtually be preserved by several options within each logand. Logands, of course, take their place on the ladder close above micro-commands, between these and machine-instructions. By their composition, logands are, however, generic portions of machine instructions, not merely program building-blocks. To distinguish it from a machine-language subroutine, a sequence of logands which performs one machine instruction is termed a logic program or LOGRAM, for short.


COMPUTER COMMAND ABSTRACTION LADDER
NATURAL HUMAN LANGUAGE
"PIDGIN" LANGUAGE
MACRO COMMAND
INSTRUCTION
LOGAND
MICRO COMMAND
MACHINE LANGUAGE
IF (ABSF(X(I))-ABSF(Y(I)) 9, 12, 11
Meaning: If the absolute value of the function . . . . . etc.
SINE, X, Y
Meaning: Cause a sine computation subroutine to obtain the argument from the storage cell at address X and to place the resulting function in the storage cell at address Y.
ADD A
Meaning: Add the contents of the storage cell at address A to the contents of the machine's accumulator register with sign control and overflow indication.
ab, pip, em
Meaning: Move the contents of register A into register B, increment the contents of register P by one, move the contents of register E into register M.
em
Meaning: Move the contents of register E into register M.

The AN/UYK-1

Ramo-Wooldridge, believing that the Stored Logic concept is one of today's promising developments of computer practice, had used a form of this concept in the design of a very economical, yet sophisticated, small-scale machine. The Intellectronics Laboratories of Ramo-Wooldridge recently announced this modern, solid-state, parallel binary, digital computer with stored logic characteristics and capabilities. Designated the AN/UYK-1, it was developed under the sponsorship of the Bureau of Ships to serve as a rugged and adaptable shipboard computer. The AN/UYK-1 has a basic 8192 15-bit word core memory expandable to 32,768 words. Its simple circuitry mechanizes only logands, albeit 46 types of these, with 32 addressing and counting options each, or over 1400 "clusters of micro-commands" with which to set up almost any desired stored logic configuration.



On recalling the article, "A Customizable Computer," by R. L. Patrick, that appeared in Datamation, volume 6, number 3 (May/June 1960), page 44, one may well feel that the Stored Logic concept amply fulfills Mr. Patrick's wishes for a new approach to practical user computing, and that the AN/UYK-1 closely approximates Mr. Patrick's hypothetical customizable computer. In some significant respects, the AN/UYK-1 offers even more than is required of that hypothetical machine. One of the characteristics of Mr. Patrick's computer is the replaceable logic plate. This improvement is a crucial one, since it enables the user to select his logic, but it limits itself to making the general-purpose interpreter a part of the hardware, insofar as the programmer is concerned. The small compact plate constitutes a very fast "fixed storage" component with logic to be altered only by manual installation of another plate. The language of the computer, of course, remains fixed for the duration of the program. In the light of the usual rigidity and slowness of interpretive systems, the user will have to admit to being well served by the changeable logic plate. In fact, even a somewhat less flexible method of setting the logic of his machine, a method by which the user is provided with permanently wired logic cards for subroutines, would be a long step ahead.

The AN/UYK-1, however, goes further. For additional flexibility, its logic is put under program control. In the AN/UYK-1, the user can "read in" the logic configuration of his choice, and can alter it by changing a few words of basic storage, even during the running of a program. The AN/UYK-1, in keeping with the Stored Logic concept, has variable instruction list and format without a corresponding hardware requirement. Consequently, it adds economy of space – and money – to the vast economy of time obtainable from Mr. Patrick's small-scale, large-capacity computer.

machine description

Since, the Stored Logic concept may be especially useful to the practical user who is likely to operate his computer by direct access, it seems very appropriate that the concept be first put to work on a small scale. The AN/UYK-1 is only 59 by 20 by 14 inches in size. Viewed as an information processing system, the AN/UYK-1 is designed for tasks in scientific analysis, data reduction, and similar applications. It also meets the requirements of a satellite computer to a large unit.

The AN/UYK-1 has six accessible flip-flop registers, an adder, an address counter, a parameter counter, a carry indicator, and an over-flow indicator. The elemental fixed word-length of the machine is 15 bits. The word-length is similar in nature to the 6-bit elemental length, usually called a character, in a so-called variable word-length machine. The stored logic interpretive mode, typical for the AN/UYK-1, permits the use of a variety of word-lengths, particularly multiples of 15 bits.

Memory access time is 6 microseconds. In internal binary operation, the AN/UYK-1 uses base-complement arithmetic. The basic logic 15-bit add time, including access, is 12 microseconds, the duration of one direct-address logand. A fixed-point multiply operation on 30 bits, in the interpretive mode, takes 561 microseconds. Floating-point arithmetic with, for instance, a 15-bit fraction and a 15-bit exponent, as well as binary-coded decimal character operations, are merely regarded as alternate word-length modes in stored logic work. Multiple-length arithmetic is greatly facilitated by the handling of the carry between words through a multiple-option add command structure.

The structure of the logic command, or logand, is that of either a single-address or a no-address 15-bit word. One type of logand is composed of a 6-bit primary command, a 5-bit option field which contains flags for memory access, sequence counting, and addressing mode options, and a 4-bit secondary command. Another type of logand has a 3-bit option field and a 6-bit secondary field containing a parameter or one of 64 addresses in the "scratchpad" portion of memory. The rest of the memory is reached by optional indirect addressing, usually through a word stored in the directly accessible registers.

modes of use

The logic of mechanizing logands, and only that logic, is built into the hardware of the AN/UYK-1. In one mode of use, programs may therefore be constructed directly

from logands, and ordered sequences of logands stored in memory exactly like conventional program instructions. The principal purpose of the Stored Logic concept, however, is to produce a fast, practical interpretive programming format. In order to clarify the nature of the special interpretive mode offered by the AN/UYK-1, and the difference, to the user, between the two approaches, it may be worthwhile to discuss each of them.

First and foremost is the approach taken by the "casual" programmer for whom any required logic package is prepared and stored in memory. He then deals with an interpreter exactly suited to his needs. The special affinity of the AN/UYK-1 for interpretive work considerably reduces the usual loss of efficiency of machines in which the effective computing speeds in an interpretive mode are much less than their memory access times would suggest. On the AN/UYK-1, the practical user writes macro-instructions, the execution times of which are within a few milliseconds. A 30-bit arithmetic square-root instruction, constructed from some fifty logands, for instance, may take about 5 milliseconds. Individual macro-instructions are, of course, based on lograms constructed quite independently from one another within the logic package. Single lograms can easily be replaced and new macro-instructions made available to the user. The flexibility of logram control offers desirable programming features. The characteristic command language of any computer can be made to instruct the AN/UYK-1. The number of addresses in an instruction can be made to depend on the type of instruction, e.g., three addresses for arithmetic, two for transfers, one for shifts. The concept of program interchange among computer user groups may also be boosted by these propensities.

In the usual interpretive system, the pseudo-instructions are designations of subroutines and of the data on which these are to operate. The interpreter routine itself picks up each pseudo-instruction, interprets it to identify the subroutine and the data demanded, and transfers control to the subroutine. At the conclusion of that subroutine, results and control are returned to the interpreter, which then moves on to the next pseudo-instruction. In order to enable the subroutine to return control to the interpreter, the interpreter must also remember the location in the program where the call for that subroutine was issued. The AN/UYK-1 is run interpretively without the usual interpreter routine. A counter is merely passed from logram to logram, as it sequences through macro-instructions. Each logram picks up this counter to find its data, advancing the counter in the process by the number of data locations pertaining to that logram. The last data location designates the next logram, to which control is directly transferred.

The arrangement of micro-commands to make up the building-block logands is such that the stepping of counters is performed together with useful operations, and as a concomitant of certain addressing commands. Such a logand as "obtain the address of a piece of data from an instruction, obtain the data itself, increment the logand counter, and increment the data-address" (mnemonic: LEIP) is carried out in 18 microseconds. Those parts of a logic program which are concerned with the necessary linkages thus benefit significantly from a "built-in" interpreter. Examples of much simpler logands are "shift the contents of the accumulator n places and increment the logand counter" (duration 12 plus 3n microseconds), "exchange the contents of the p-register and the a-register and increment the logand counter" (duration 12 microseconds.)

Among the software aids that are put at the disposal of the practical user is a Symbolic Program Assembler (no acronym contemplated) which takes charge of locating the required lograms in memory in accordance with the information contained in macro-instructions written by the user. Other essential pieces of software that go with the AN/UYK-1 as used in the described modes are utility and diagnostic routines and a Logram-Assembler that accepts logands in symbolic code and turns out machine-coded lograms.

This last routine, of course, is meant as an aid to the exceptional user, or to the programming specialist who will actually prepare the lograms or use the machine at the basic logand level.

The second mode of use is not seen, on the AN/UYK-1, as a necessary machine-language method for those who, for various reasons, are opposed to interpretive work. This mode of use is offered as a license for specially interested people to reach into the logic structure of the machine for sub-instruction-level use, somewhat similarly to the way in which, on some machines, light displays of memory contents and aids to intervention in information transfers are accessible only to those specially interested.

Among the numerous logic commands, or generic machine instruction portions, with their multiple options, there are some, such as extract, block transfer, table lock-up and inter-table match operations, which should please the dedicated programmer. There are also many Boolean algebra operations and conditional skip and branch instructions responsive to 16 specified conditions. The logic-command programmer is compensated for extra labor by an appreciable bonus in machine speed, but it should be evident from the facts and discussions above that the interpretive speeds obtainable by the casual programmer are still high enough to preclude any necessity for him to abandon his easy program form to work with the logands themselves.

further details and conclusions

The design criteria of the AN/UYK-1 are based on military specification requirements. The AN/UYK-1 housing consists of an aluminum casting. This casting is in two pieces, allowing front access to all power supplies mounted in the rear section, and all insert circuit cards mounted in the forward section. Self-checking capabilities are provided within the machine.

The AN/UYK-1 is synchronous, with pulses occurring every 3 microseconds. Most of the logic commands of the machine are carried out either in four clock pulses, under direct addressing option, or in six pulses, under indirect addressing option. The electrical power requirement of the AN/UYK-1 is less than 1 kilowatt of 115 volt AC, 60-400 cycle flow. External air conditioning is not required, since the computer dissipates very little heat and contains its own cooling system.

The speeds of the AN/UYK-1 memory access and internal operation are in a class with that of much larger equipment. While computers in its own class often are expected primarily to process information in small units and requiring only logic operations and some relatively simple arithmetic, the AN/UYK-1 can economically do work in which it performs sequences of program steps simulating a single instruction of a larger machine. The effective speed of such interpretive work is high enough to warrant use of the machine in many fields of application.

As a satellite system component, the AN/UYK-1 can offer its internal binary nature, high internal speed, and instructions for manipulating tables and flow-chart logic, such that it could perform, for the central computer, some arithmetic in floating binary, data input and output control work, data retrieval, and assembly or compiling operations.

The "practical user" will undoubtedly write the history of the Stored Logic concept, its uses and extensions. It is anticipated that he will find the AN/UYK-1 able to implement this concept effectively.

CIRCLE 116 ON READER CARD

An editorial commentary on

THE GAP IN PROGRAMMING SUPPORT

by **ROBERT L. PATRICK**
Computer Specialist, Manhattan Beach, Calif.

THE trend towards higher level programming languages is on the upswing. These languages have a certain appeal in the marketplace, and if they are done well and adequately supported in the field, will definitely sell machines.

At the same time, those persons who predict the growth of the field and keep statistics on numbers of machines installed, indicate that we are only beginning to scratch the surface of the market. Supposedly that market, as it is developing, will be large enough for all competent manufacturers to obtain and hold a significant piece. Again, as it has been stated many times before, it appears as though the hardware types are outstripping the programming types. In short, the lead time on a machine is about the same as the lead time on a good textbook on programming, and is much less than the lead time on a trained installation manager. We find the limited manpower of the "profession" being spread thinner and thinner as new machine installations spring up and present machine installations are pirated in order to staff new shops. There are significant numbers of fair sized machine installations where the most senior man has only two years experience in the field. Unfortunately, it appears as though this situation will get worse in the next several years before it gets better.

This bright new future and rosy trend can continue only as long as we are able to support our machines in the field with at least some experienced programming and maintenance talent. We are all fairly aware of the problems in acquiring experienced programming talent and how we have had to go to user clubs in order to try and pass information adequately from installation to installation. There is still nothing significant coming from the universities and there is still a great shortage of proficient machine oriented programmers. While this area receives much attention and much is written about it, the problem of maintenance in the field is just as deserving of attention and is a major cause of concern.

In the past several years, the hardware has increased magnificently in both reliability and speed of operation. While the programmers have proceeded on a tangent or two, there has been noticeable progress in the programming of machines and the definition of new applications. On the other hand, nothing significant has occurred in the area of field diagnostic programs for at least ten years. Self-checking diagnostic programs accompanied the very early machines, as did customer engineers who were inadequately trained in the manipulation or improvement of these programs. Although our machines have improved in the past few years, the diagnostic packages have not. We joke about a computer having the ability to "learn" the diagnostic routines, and to still be in bad order even though the diagnostics will run. There is some measure of truth in this since customer engineers have always been limited in their ability to maintain equipment to those troubles they can define and locate.

Early installations extracted themselves from this dilemma by establishing ad hoc teams of programmers and maintenance men to pursue elusive maintenance bugs. The Chief CE and the Senior Programmer would together explore the machines "inards" and, after appropriate diagnostics, would operate on the beast in hopes of curing him. Each of these men had confidence in the other. Quite often the Senior Programmer would be called upon to help some junior programmers who kept crying "machine, machine" when it was really an obscure programming bug.

As the field has progressed and enlarged, the ranks of customer engineers are decimated by promotions as are the ranks of senior programmers. On top of this, we have no new senior, machine oriented, programmers coming along (due to the emphasis on higher level languages). The situation is steadily deteriorating.

In the past, the testing of components under extreme conditions would cause an intermittent or transient bug to show up solidly and hence it could be repaired. With the newer circuits and more reliable components, tests of this type are no longer applicable, but we have yet to find a suitable substitute.

Since the days of the disposable main frame are not quite here, something must be done. The machines must be maintained in the field and specialists are in short supply. It seems up to us, who are directly associated with the field, to become alarmed about this problem before it becomes critical and to take some active steps toward a solution.

It seems some strides have been made in the art of pattern recognition in the past few years. We see in the journals and papers presented at conferences that pattern recognition techniques are inching along and have been quite successful in certain limited areas. One striking area is the mechanized pattern recognition as is used in the MICR banking systems.

At the same time, we see and hear several manufacturers discussing how they have used computers to help design their next product. There are even manufacturers who proudly inform us that they have used ancillary computers to determine the power loading and current requirements on each pin of a large system. There are other manufacturers who have gone a step further and who have used supporting computers to determine even the routing of the backpanel wiring so as to achieve minimum cross talk while achieving maximum packing density. The output of these programs are updated wire lists on magnetic tape, printed wire lists for manual wiring, and in some cases punched cards or punched paper tape to control a tape controlled machine which is a "wire rat that runs the maze of the backpanel so as to automatically wire a chassis directly from computed output". The field has advanced sufficiently so that these things are done only with human supervision and without human intervention.

I wonder if perhaps we could bring these two techniques together so that we might solve our maintenance dilemma. For the first time we have schematics of the computer in machine readable form. Perhaps we could develop a program which when given the symptoms of a failure and the final results of the happening could look for failure patterns and come up with an answer that either indicated an insufficient sample had been supplied and no recognizable pattern existed, or an indication of one or more possible hardware conditions which could have caused the error to take place.

I wonder if anyone other than myself is concerned about the problem. I wonder if there are some bright boys buried in the bowels of some gigantic corporation who are working on the problem. I wonder if we **could** build a dynamic diagnoser. I wonder . .

CONTROL DATA'S NEW

160-A: LARGE-SCALE COMPUTER FEATURES

Uses the same basic circuits as the Control Data 1604. Includes the following features previously found only in large-scale computers:

- buffered input/output
- interrupt
- expandable memory (8192 to 32,768 words)
- special powerful instructions

160-A: SYSTEM EXPANDABILITY

Can be expanded from a minimum system up to full system capacity—including electric typewriter, magnetic tape system, card reader/punch, and line printer. The Control Data 350 Paper Tape Reader and the Teletype Paper Tape Punch are standard equipment.

160-A: SPECIAL USES

Control Data Satellite Computer System. The 160-A can be used as a satellite computer with direct access to the large-scale 1604.

Microwave Communications. The 160-A can be used to communicate via microwave link with the large-scale 1604 at transmission rates of approximately 1,000,000 bits per second.

160-A: RANGE OF USES

A general-purpose computer, the 160-A can be used for an almost unlimited number of applications. With its buffered input-output, expandable memory, interrupt, high speed, and special powerful instructions, the 160-A can handle a variety of computing applications in

- commercial data processing
- engineering problem solving
- off-line data conversion
- scientific data processing
- real-time data acquisition/data reduction

160-A: HIGH-SPEED CIRCUITRY

Using all-transistorized circuitry, the 160-A executes 60,000 instructions per second. Memory cycle time is 6.4 millionths of a second; access time is 2.2 millionths of a second.

160-A: COMPATIBILITY

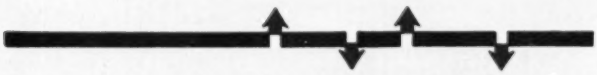
Programs written for the Control Data 160 can also be used with the 160-A. All peripheral equipment used with the 160 can likewise be used with the 160-A.

V 160-A COMPUTER

Buffered Input-Output

Input-output operations are carried out independent of the main computer program. When the transfer of input or output data is required, the main computer program is used *only* to initiate an automatic cycle which buffers data to and from the computer memory. The main computer program then continues . . . while the actual buffering of data is carried out *independently and automatically*.

Interrupt



The 160-A periodically senses the input-output channels for the presence of an interrupt signal. When an interrupt is detected, the program jumps to an interrupt sequence in memory . . . which includes the instructions necessary to return to the main program at the proper place. An interrupt is not recognized during a non-buffered input-output operation.

Powerful Instructions

Included in the 160-A repertoire of 91 instructions are special instructions usually found in computers much larger than the 160-A. Some of these are:

- **STORE CONTENTS OF P** – which gives the programmer the option of storing the address of the instruction which is currently being executed.
- **RETURN JUMP** – only one instruction is required to store the return address in the subroutine and at the same time jump to the entrance of a subroutine.
- **KEY CONTROL STOPS AND JUMPS** – provide optional operator-initiated sequence controls.

Expandable Memory

The 160-A basic memory consists of 8192 words of magnetic core storage contained within the desk-size cabinet. Additional external memory modules of 8192 words each can be added up to a maximum of 24,576 . . . for a total memory capacity of 32,768 words. The internally stored program switches from one memory module of 8192 words to another, depending upon the addressing mode.

CONTROL DATA CORPORATION
MINNEAPOLIS 15, MINNESOTA

CIRCLE 38 ON READER CARD

National*

Presents opportunities for personnel qualified for the following openings located at Dayton, Ohio

RESEARCH & DEVELOPMENT

DATA TRANSMISSION ENGINEER: For advanced planning in ON-LINE REAL TIME SYSTEMS. Applications would generally be focused on large-scale business and finance operations. Appropriate engineering degree and 6-10 years of experience necessary.

ELECTRONIC ENGINEER: Openings in commercial or military R & D up to staff or project level. Circuit and logical design utilizing advanced concepts. B.S. Degree plus experience necessary, M.S. preferred.

SYSTEMS ENGINEER: B.S. or M.S. in Electrical Engineering with interest in development of business machine systems with 3-6 years of experience which should include some advanced circuit design preferably for Computer Development, but other may suffice.

COMPONENTS ENGINEER: B.S.E.E. experienced in component evaluation and working with vendors. Familiar with transistor type circuits.

All openings are located at Dayton, Ohio.

ELECTRONIC DATA PROCESSING

SYSTEMS AND SALES

CUSTOMER SITE REPRESENTATIVE: Locations will vary. Qualifications require broad experience in programming, operation and systems analysis. Must have worked with tape systems and be familiar with computer-user problems. Training given at Dayton prior to installation assignment.

SALES SUPPORT: At least 3-5 years of programming experience plus B.S. or M.S. in Business Administration or Mathematics will qualify for challenging work with EDP sales organization. Opportunities are varied and include:

Programming
Manual Writing
Systems Analysis
Programming Research
Programming Instructor

PROGRAMMERS: The NATIONAL line of EDP systems including the 304, 315 and 310 provides the basis for interesting and effective work in any operation wherever money or merchandise is handled. Stability and growing responsibility are characteristic of the climate at NATIONAL whether your work is in one of our Data Processing Centers or with our Data Processing Systems and Sales group in support operations. General qualifications for present openings are a college degree and experience with a tape system applied to business or financial functions.

CENTERS

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Dayton
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NATIONAL'S newest contribution to the business field is its modern and complete data processing centers. These centers, no matter where they now exist or where they will exist in the future, answer the everyday needs of the small or the large business in the area of electronic data processing. To fulfill this function—service to business—we need men of above-average ability who are trained and experienced in tape system computer programming or operations. In most cases, a college degree is preferred.

For these and other professional level opportunities in challenging areas of work, write to:

T. F. Wade, Technical Placement G14,
The National Cash
Register Company,
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Dayton 9, Ohio

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ELECTRONIC DATA PROCESSING
DIVERSIFIED CHEMICAL PRODUCTS
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CIRCLE 77 ON READER CARD

DATAMATION *news briefs*

601 SYSTEM READIED FOR RCA COMMUNICATIONS

Many of the techniques and much of the equipment in the RCA 601 will be employed in a new electronic system scheduled for the east coast headquarters of RCA Communications, Inc. The system is intended to solve the critical problem growing out of increasing radio and cable traffic.

The system will be able to handle traffic transmitted by wire lines, microwave, coaxial cable, high-frequency radio, tropospheric scatter propagations, and satellite communication systems. A series of checkup data, known as parity bits, will be transmitted along with the message; should the final content vary in any way from the original, the parity bits, functioning as detectives, will request correction.

The system is equipped with buffers to quicken incoming messages to speeds acceptable to the computer and then to slow them down to what the outgoing transmitter can accomodate.

NATIONAL DP SERVICE FORMED IN PHILADELPHIA

Associated Data Center, Inc., the only national organization of independent data processing service companies, has been formed in Philadelphia. Roger B. Gregory has been named president. A. D. C. services include all types of data processing from basic punch card to large scale computer programming and processing. Affiliated companies are: Electronic Data Processing Corp.; Punched Card Services Inc.; Tabulating Services Co.; Malt & Ness; Data Processing Services; American Tabulating Co.; Data Computing Service; Machine Accounting Inc.

CIRCLE 100 ON READER CARD

CDC 1604 AT SCRIPPS & U. OF WISCONSIN

The largest memory capacity of any university computer installation in the nation, 1,500,000 binary digits, is contained at the Control Data Corp.'s 1604 installation at Scripps Institute, La Jolla, Calif. A 160 is used as a data preparation unit, making the facility similar to the one recently acquired by the University of Wisconsin at Madison. The Scripps system, which includes eight tape units, will be engaged both in data reduction and scientific work for the Institute. At Wisconsin, a similar system will be available to all academic departments of the University.

CIRCLE 101 ON READER CARD

COMPUTING RECOMMENDED FOR SECONDARY SCHOOLS

Fred Gruenberger, The Rand Corp., Santa Monica, Calif., recently addressed the National Council of Teachers of Mathematics' annual convention in Chicago on the topic of "The Introduction of Computers to Secondary Schools." His talk was illustrated with a demonstration on a 1620 operated in synchronization with his address. Gruenberger brought forth four points concerning a computer's function in a secondary school. He stated that it will aid in traditional work now being done; bring college problems to a high school level; lead more students into research; and finally, provide some "fun work" for students interested in mathematics.

B-L'S DATA SERVICES OFFERS UNIQUE DP

Benson-Lehner Corp. has expanded its subsidiary corporation, Data Services Inc., with complete and somewhat unique automatic and semi-automatic data processing facilities located in Washington, D.C. and Santa Monica, Calif. Some of the services being offered include film, strip chart, circular chart or oscillograph record reading; graphical plotting services including line drawing and point-by-point plotting; report preparation and tabulation and computer services. Both facilities were in full operation on April 1. John Sayer is Data Services' eastern manager and Walt Brown, Jr., is in charge of the western operation.

CIRCLE 102 ON READER CARD

STRETCH DELIVERED AT LOS ALAMOS

Shipment of IBM's first STRETCH computer from Poughkeepsie to Los Alamos, was completed late last month. Under development for five years STRETCH will be utilized for research in nuclear and thermonuclear energy, including weapons, rocket propulsion and medical research. Heart of the system is the central processing unit (right background). In the foreground is the operator's console.

MOBILE CENTER FITTED FOR UNIVAC 90

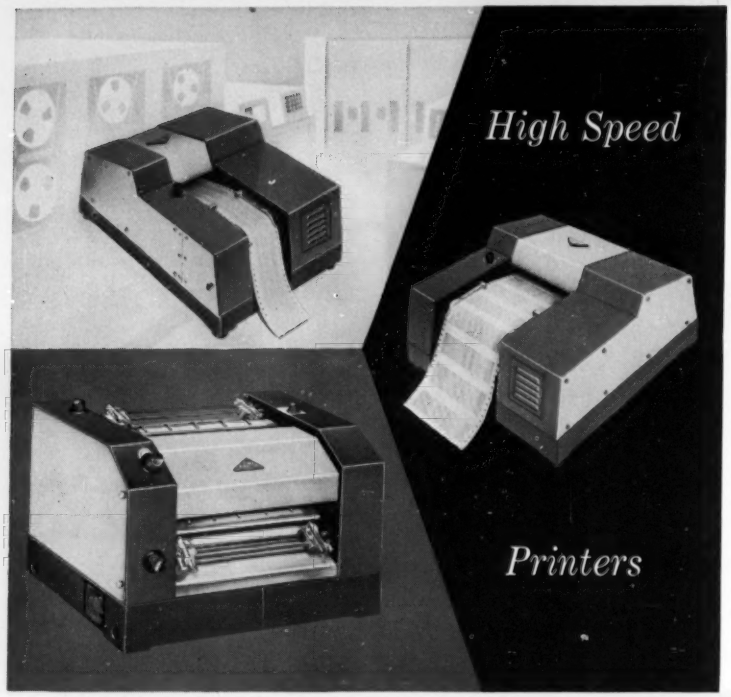
Univac Division of Sperry Rand Corp. has gone on the road with a Mobile Computer Center designed for doorstep customer service. It is fitted with a Univac solid-state 90 system. The tour, which may top 25,000 miles, will offer customers who lack computer room capacity for two systems an opportunity to maintain operations simultaneously with the changeover. The systems include a central processor with a 50,000 digit internal memory, a 600 line-a-minute printer, a 450 card-a-minute reader and a 150 card-a-minute read-punch unit.

CIRCLE 103 ON READER CARD

AMERICAN SYSTEMS HAS EDP DIVISIONS

American Systems Inc., Hawthorne, Calif., has established seven new op-

Completely Redesigned



by

ANELEX®

. . . of course

Data processing systems builders* . . . and users expect this from Anelex. And for good reason. Most new developments associated with high speed line printing for EDP systems . . . even to high speed printing using machine-recognizable characters . . . have orginated with Anelex.

The highly specialized skills acquired by Anelex engineers in the creative development of advanced systems enables them to best design mechanical, electro-mechanical and electronic out-put equipment. In all probability the techniques required for your particular system have already been accomplished. This group, with their extensive knowledge and experience, is available for a discussion of your requirements.

***Anelex High Speed Printers are supplied as standard equipment by 22 major computer and systems builders.**

ANELEX

Anelex printers will be displayed in Booth 93-94 Western Joint Computer Conference.

ANELEX CORPORATION

150 CAUSEWAY ST., BOSTON 14, MASS.

CIRCLE 31 ON READER CARD

NEWS BRIEFS . . .

erating divisions, some of which previously existed as laboratories. They will be known as the Information Sciences Division; Instrument Division; Component Division; Instruction Division; Electromagnetic Systems Division; Command and Control Division; and Research Laboratories Division.

Appointed as director of the Information Services Division was Dr. Robert E. Fagen. The activities of the division encompass mathematical and statistical research, computer programming and the development of computer programming systems, computation services, digital system studies, logical design, and advanced system analysis.

CIRCLE 104 ON READER CARD

MOSHMAN APPOINTED '61 EJCC CHAIRMAN

Dr. Jack Moshman has been selected conference committee chairman of the 1961 Eastern Joint Computer Conference scheduled for December 12-14, Washington, D.C. He is a vice president of C-E-I-R, Inc., Arlington, Va. Bruce G. Oldfield, IBM Federal Systems Division, will be chairman of the program committee. Vice chairman is William L. Witzel, also of C-E-I-R. Herbert R. Koller will be secretary of the conference. Oldfield has already issued a call for papers. Deadline for submission of abstracts and summaries is June 20th.

✓A data processing spare parts documentation service for technical engineering service firms and manufacturers of military systems and equipment has been created by The Service Bureau Corp., N.Y.C.

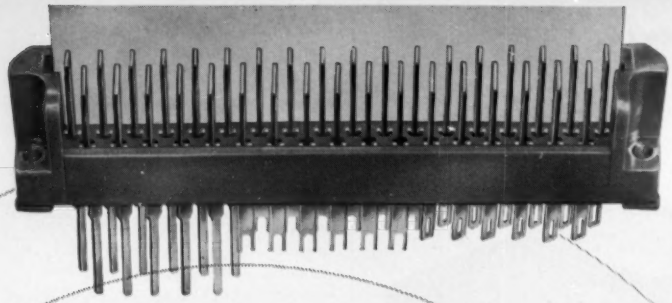
CIRCLE 105 ON READER CARD

✓Computer Usage Company, Inc., a computer services firm, has moved to larger quarters at 1825 Connecticut Ave., N.W., Washington 9, D.C. The firm, with headquarters in New York, opened its Washington facilities in August, 1959.

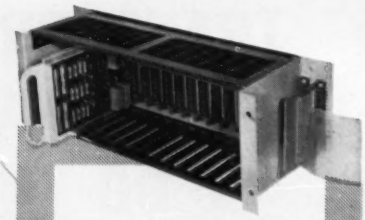
CIRCLE 106 ON READER CARD

✓An expected attendance of over 2,000 is anticipated for the 16th National Conference of the Association for Computing Machinery, Statler Hilton Hotel, Los Angeles, September 6-8. An estimated 50 exhibits is expected for the annual show and conference.

✓Users of the Honeywell 800 have formed a users group called the H-800 Users Association. John J. Koerner was elected to a two year term as president, and Raymond E. Harbaugh was



WHY DID WESTINGHOUSE SELECT ELCO VARICONS FOR PRODAC*?



Because WESTINGHOUSE found our VARICONS permit "rapid, easy removal and replacement and yet provide the reliable, constant contact so necessary" to their PRODAC Digital Computer! Hence you will find VARICON Series 7001 35-contact models and our VARIPAK Series 9006 printed circuit card enclosures throughout these remarkable computers. Shown, top left, is that VARICON Series with various types of terminal ends available; and at the upper and lower right, VARIPAKS illustrating flexible cable VARICON applications. You will also find most major computer manufacturers relying upon the reliability of these ELCO products.

So why not solve both the design and reliability problems of your own most sophisticated packaging project by writing for our Bulletins 7001 and 9006 now while it's on your mind!

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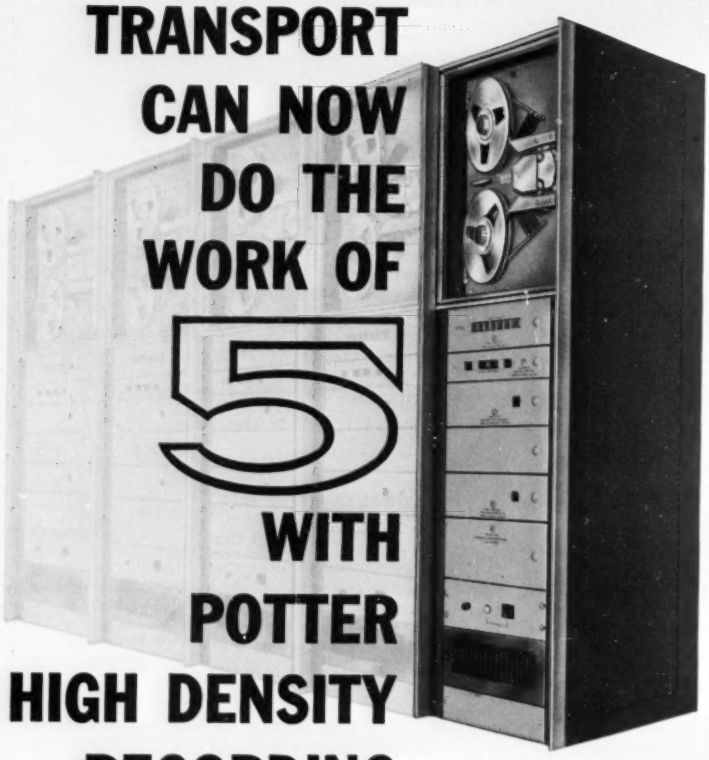
CIRCLE 39 ON READER CARD

1 TRANSPORT CAN NOW DO THE WORK OF 5 WITH POTTER HIGH DENSITY RECORDING



With the revolutionary new Potter High Density Recording System, one tape transport has the capacity of 5 or more conventional transports.

For highly reliable computer applications, Potter High Density Recording can give you data transfer rates of 360,000 alpha-numeric characters per second, at densities up to 1500 bits per inch on 1-inch tape. Sixteen parallel channels can be accommodated on one-inch tape. Because Potter has made the information channels self-clocking, no separate clock channel is needed, and multichannel data can be read out in true parallel form, despite interchannel time displacement.

In production units delivered by Potter for the BENDIX G-20 COMPUTING SYSTEM at the Carnegie Institute of Technology, this dramatic new technique makes recording so reliable that in 40 hours of continuous operation less than 2 seconds re-read time are required to recover information lost through transient error. Dropouts are fewer than 1 bit in 10 billion at 1100 alpha-numeric characters per inch. More than 20,000 passes of the tape can be made without losing information or significantly increasing the reading error rate.

Tested and proven in computer systems, Potter High Density Recording is presently available in the Potter 906II High Speed Digital Magnetic Tape Handler, and will be available in other Potter Tape Systems.

Write today for details on how High Density Recording can be applied to your data handling problem.

POTTER INSTRUMENT COMPANY, INC. • SUNNYSIDE BOULEVARD, PLAINVIEW, NEW YORK

CIRCLE 32 ON READER CARD

NEWS BRIEFS . . .

elected vice president. The next meeting will take place in Houston, October 26-27.

CIRCLE 107 ON READER CARD

✓The Federal Reserve Bank of Boston has placed an NCR 304 into operation handling checks and other banking functions. Pre-punched government checks can be processed by the 304 system's card reader at the rate of 2,000 a minute – 20 times faster than present mechanical equipment. The bank handles an average of 150,000 of these checks a day.

CIRCLE 108 ON READER CARD

✓Remington Rand Univac, has opened their new Univac Service Center in the National Life and Casualty Building, Phoenix. The new center offers the Phoenix area time on a per hour basis of a Univac solid state 90 and related peripheral tabulating equipment.

CIRCLE 109 ON READER CARD

✓Jefferson Medical College has enrolled 43 faculty members in a special course in programming at the computing center of The Franklin Institute, Philadelphia. College administrators hope to make use of data processing in such applications as student evaluation, rostering, and financial accounting.

✓Minneapolis-Honeywell's Electronic Data Processing Division has developed converters that automatically translate records on magnetic tape from IBM and Univac language into Honeywell language. The translations proceed at whatever speed the non-Honeywell tape reads recorded data. Translations, it is claimed, often result in a running ratio of two and one half non-Honeywell tapes to one Honeywell tape.

CIRCLE 110 ON READER CARD

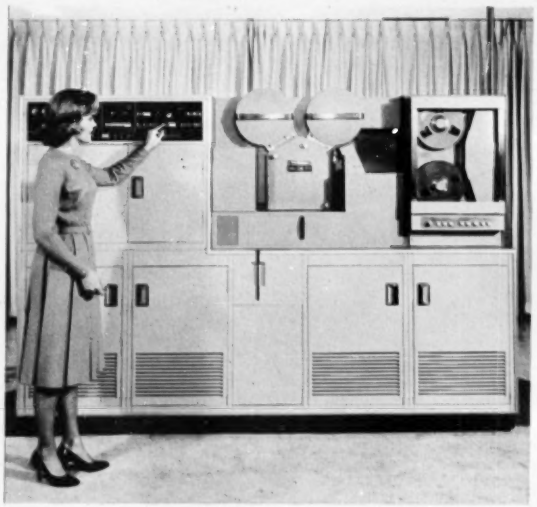
✓The 7070/1412/1401 combination at The Wilmington Trust Co. is the first of its kind to be delivered by IBM. Programs for the first uses of the machines in the bank's checking and savings deposit accounting, and commercial and consumer loan operations already have been assembled and successfully tested.

CIRCLE 111 ON READER CARD

✓March 31st marked the tenth anniversary of the operation of Univac I serial number 1, the first commercial electronic computer system, by the Bureau of the Census, U.S. Department of Commerce. First used during the final stages of the 1950 Census tabulations, Univac I has been in almost constant use, a spokesman stated.

24,000 characters per second

DACOM HIGH-SPEED PRINT-OUT



A HIGH-speed computer print-out equipment line, known as the DACOM system, will convert information from magnetic tape into plain language or microfilm at speeds up to 20,000 characters per second.

Produced by Recordak, the system can reproduce a complete page of data, containing as many as 8,064 characters, in approximately one-half second, in a single 16mm microfilm frame. Any desired background format, such as statement, bill, or accounting forms may be optically combined with the output of information so that the data can be produced in final finished form.

Peripheral equipment for on-the-spot high-speed film processing, and for continuous or selective hard-copy facsimile production from film, is also to be available in addition to visual film reference work stations, in order to provide a maximum of practical advantage and verstaility.

The system is designed for use with magnetic tape having 7-channel binary code format. It accepts directly data recorded at 200 characters-per-inch, 75 in./sec. The system is designed to be used with one or two magnetic tape units having IBM compatible heads and modified to accept IBM reels. Two tape drives are desirable to save tape loading and rewind time.

Point-plotting can also be accomplished with the DACOM system photographically and at high speed. No overlays or descriptive labeling are required. Descriptions are automatically recorded by the system, which can vary between the plotting mode and typewriter simulation at a sustained speed of 15,000 characters per second.

The control units provide synchronization for the three elements of the system – the tape drive, the cathode ray tube display unit and the camera.

CIRCLE 113 ON READER CARD

MATHEMATICIANS

At MITRE, mathematics provides solutions to a variety of complex problems in the development of computer-based electronic systems for command and control of aerospace forces, weapons and vehicles.

Mathematicians with broad interests in analytical methods and techniques, and an appreciation of the complexities of system work find professional satisfaction in conducting studies which will lead to new and unique systems. MITRE offers a unique environment in which to apply professional abilities in such diverse areas as:

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A brochure more fully describing MITRE and its activities is available upon request

CIRCLE 78 ON READER CARD

Ampex's second-generation TM-2 uses design principles already proved the hard way—*in on-site computer use.* And with these proved principles, it gives performance far exceeding any available industry standards: tape speed to 150 ips; closely controlled 2.0 ms start/1.5 ms stop times; up to 200 Kc net character transfer rate (1" tape). *Ampex* **performance standards** *set the pace in maximum system thru-put.*

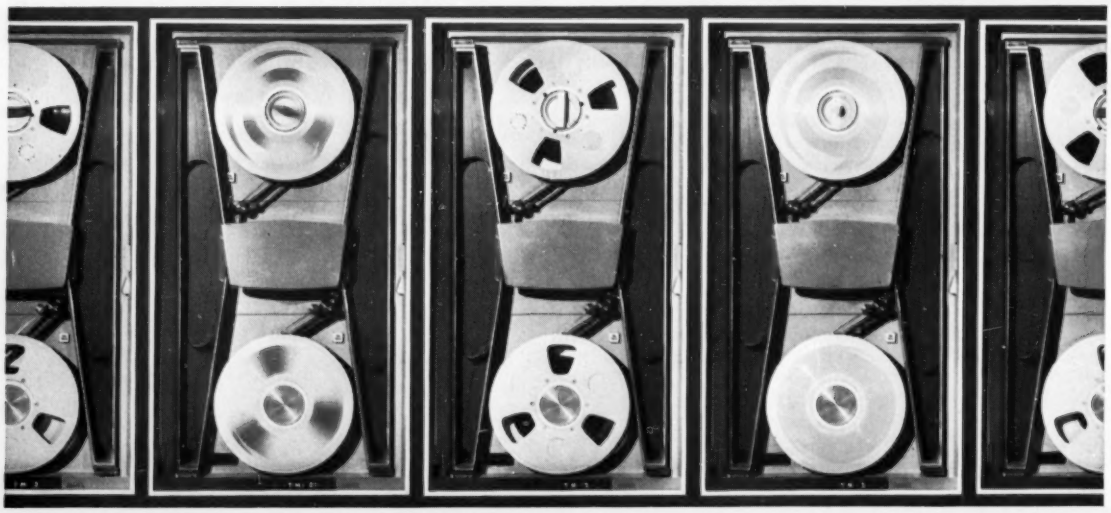
Ampex—the world's largest corporation devoted solely to magnetic tape technology—has sold over 3,500 digital tape transports. Experience encompassing design, development and production of virtually every type of head and tape transport has evolved the present use-proved principles. Fifteen of the world's leading computer manufacturers specify Ampex because Ampex systems reflect unmatched knowledge and specialized experience, besides offering new industry performance standards and world-wide service. **User acceptance** *is the true measure of Ampex's contribution to maximum system thru-put.*

For TM-2 details and specifications please write:
AMPEX COMPUTER PRODUCTS COMPANY
TAPE UNIT DIVISION
BOX 5000 • REDWOOD CITY, CALIFORNIA

AMPEX 0/1™

$$(\text{TM-2}) = \frac{Q\,max}{\$}$$

WHERE (TM-2) = AMPEX TM-2 MAGNETIC MEMORY SYSTEM
Q = ACTUAL SYSTEM THRU-PUT
$ = MAGNETIC TAPE TRANSPORT INVESTMENT



CIRCLE 34 ON READER CARD

Decision and control in today's military and governmental structure frequently must follow almost as soon as events occur. Yet the forces involved may span continents. And the information for control of these forces may be enormous in volume. ▪ To help leaders make decisions and exert control in response to events of the moment, we at System Development Corporation have helped create a new technology based on automated information processing assistance. ▪ SAGE is in operation as the first system of this new technology. Another — the SAC Control System — is in development. And we are working on two other extremely large systems in their initial stages. In contributing to these systems we have dealt mainly with their analysis and synthesis, training men in their use, instructing great computers on which they are based — and research into future generations of systems. ▪ We have developed an interdisciplinary approach to system development. The four fields are Computer Programming, Engineering, Human Factors, Operations Research. To staff our rapidly expanding programs in Santa Monica, California, Washington, D. C., and Paramus, N. J., we are seeking scientists and engineers in these fields. Please address Mr. R. L. Obrey, 2401 Colorado Avenue, in Santa Monica.

CIRCLE 76 ON READER CARD

SYSTEM DEVELOPMENT CORPORATION

computer time broker

COMPUTER USAGE OFFERS UNIQUE SERVICE

What looks like one of the best electronic data processing ideas to come down the pike in a good many months has been turned into a going operation by Computer Usage Company of New York City. Stated simply, CUC has become a computer time broker – selling time to anyone, any time they choose on the machine of their choice. How and why this operation evolved was explained to DATAMATION in CUC's offices by the firm's president, Elmer Kubie and the Computer Time Sales Division director, E. M. Chafets.

The example was cited of a firm with a program to run and no machine on which to run it. Normally, this firm would have at least two courses of action open to it. They could take their problem to a computer center or to another computer user who has machine time available. But, CUC asks, would machine time be available when the customer wanted it? Would a computer the customer preferred be available? In the case of another user, what assurance of the operator's ability to handle his work could the customer have?

CUC provides some interesting answers to these questions and therein lies the story.

Computer Usage has contracted with a large number of computer users to sell their excess machine time for them.

To the customer who wishes to buy time, Chafets can therefore offer a choice of a wide variety of computers, immediate service and a CUC operator familiar with the machine to be used. CUC suggests that customers' staff members may be needed to supervise a job but the firm is prepared to handle the complete package from initial analysis through programming to machine operation. It should be noted, too, that there are no minimum monthly rentals involved. CUC will sell you only the time you need to process your work.

In the cost department, CUC points out that the machine owner is selling idle time he cannot use and is therefore willing to sell almost at cost. Even after CUC's mark-up is added, Kubie claims that the resulting cost is far lower than any other service organization could offer.

The company has prepared special forms for the use of all parties involved. These include an installation record, console instructions and duplicate forms for the lesor and lesee marked payable and receivable.

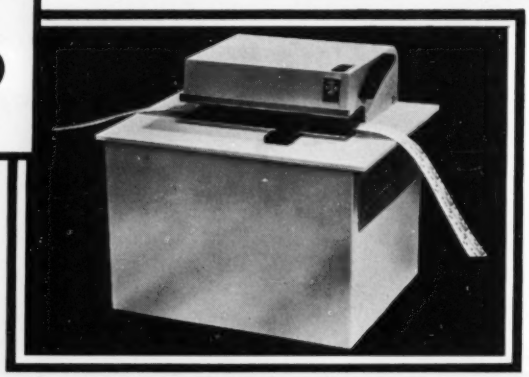
With offices in Washington, D.C. as well as New York, CUC now lays claim to the title of the largest independent analytical and programming group in the country. The firm has a staff of 70.

CIRCLE 117 ON READER CARD

CONTROL DATA

High Speed Punched Paper Tape Reader

350



COMPUTERS
BUSINESS MACHINES
DATA REDUCTION
DATA PROCESSING
MACHINE CONTROL
INDUSTRIAL CONTROL

- Unsurpassed Reliability
- Advanced Mechanical Design
- 350 Char/Sec Read Rate
- Start-Stop or Continuous Mode
- 5, 7, or 8 Level Tape
- Tape Widths: 11/16", 7/8", 1"
- Instantaneous tape width selection
- Reads all punched tape
  Paper-Plastic
  Colored-Plain
  Oiled or Non-oiled
- Complete freedom from programming limitations

The Control Data Model 350 Paper Tape Reader employs the most advanced tape controls and reading techniques. Multi-colored tapes can be read interchangeably without the need of bias adjustments, and new specially designed light guides in the reading head eliminate dirt collecting holes. The precise control system eliminates troublesome resonances and provides complete freedom from programming limitations. These and other features combined with careful attention to details and quality, result in a paper tape reader which provides new high standards of reliability and versatility.

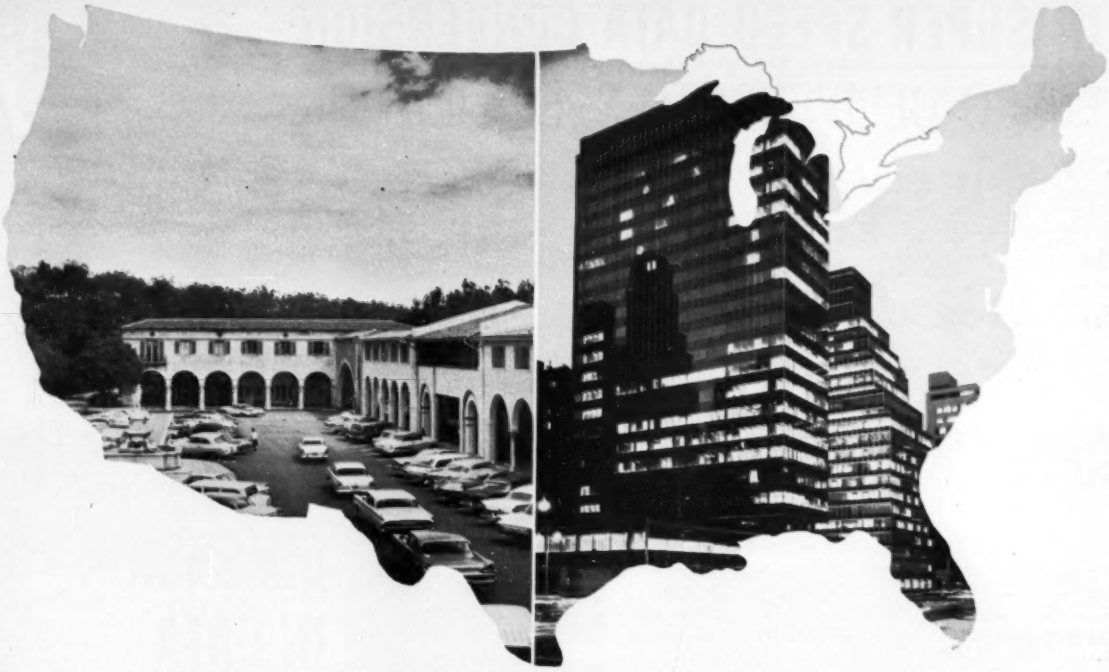
For complete specifications, prices and delivery write or call us directly or contact our nearest sales representatives.

CONTROL DATA CORPORATION

CEDAR ENGINEERING DIVISION

TWX-MP 974 • 5806 36th St. West • Minneapolis, Minn. • WEst 9-1687

CIRCLE 36 ON READER CARD



Different views . . . same viewpoint

CSC NOW PROVIDES THE SAME EXCELLENCE IN SERVICE FROM CALIFORNIA AND NEW YORK

Whether you are located on the West Coast or the East Coast—or somewhere in between—CSC offers you the same high level of professional assistance in the application of the computer sciences.

Operating out of the new California center at Palos Verdes Peninsula or the newer Park Avenue offices in New York City—an experienced CSC team can be made available to help you with your data processing or computer projects.

CSC services take many forms. Typical areas of service include:

- Analysis and Programming of Commercial and Scientific Applications
- Programming Systems
- Computer Research Projects
- Management and Staffing of Computer Installations
- Machine Feasibility Studies
- Contract Data Processing

Computer Sciences Corporation furnishes consultation, analysis, and programming in all areas of commercial and scientific data processing. Among CSC clients are such distinguished firms as Minneapolis-Honeywell, Ramo-Wooldridge, General Motors, RCA, and Southern California Edison. CSC is also available to serve you, whether you manufacture, use, or should be using a computer. A telephone call or letter will bring to your office some of the top computer talent in the country.

If you would like more information on the CSC approach to business and scientific problem-solving, write either of the offices below for an illustrated brochure.

CSC

COMPUTER SCIENCES CORPORATION

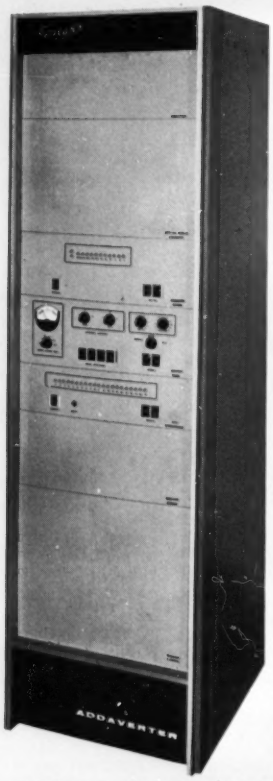
GENERAL OFFICES: MALAGA COVE PLAZA, PALOS VERDES, CALIF. • PHONE: (LOS ANGELES) SPRING 2-1179

NEW YORK DIVISION: 400 PARK AVENUE, NEW YORK CITY 22, NEW YORK • PHONE: PLAZA 2-6885

Challenging and rewarding positions exist at CSC for those who are outstanding in the computing and data processing field.

CIRCLE 16 ON READER CARD

IN SUPER-SPEED DATA CONVERSION
EPSCO DELIVERS ITS SPECIFICATION

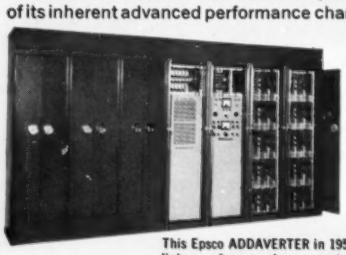


A NEW DIMENSION IN DATA PROCESSING

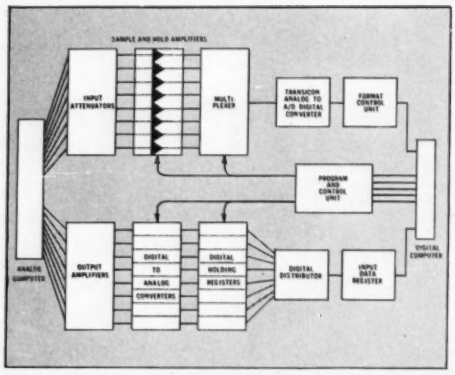
Epsco's **ADDAVERTER®** Computer Linkage Systems

The Epsco solid-state ADDAVERTER® provides on-line bi-directional communication between analog and digital computers. Computations may be shifted back and forth through the ADDAVERTER® in real time, combining the analog machine's rapid solution of complex functions with the high-speed programmable arithmetical capability of the digital machine.

The ADDAVERTER's® unmatched operational versatility is the result of its inherent advanced performance characteristics as well as Epsco's basic functional module approach. It requires no periodic calibration or peaking adjustment. A wide range of field-addable options permit adaptation to your exact needs.



This Epsco ADDAVERTER in 1957 performed the first operational on-line linkage of an analog computer and digital computer. Developed for Convair Astronautics, San Diego, this first model is still in active use today. A vacuum tube system with 10 D/A and 15 A/D channels, it provides linkage between a large-scale analog computer and either an IBM 704 or a Univac Scientific computer for simulation studies of a complete ballistic missile system.



KEY SPECS:

Analog/Digital	Digital/Analog
Input Signal Levels: ±128 V, ±100 V, ±10 V full scale models available.	Signal levels and format compatible with your digital computer.
Sampling Rate: Up to 15 KC.	Up to 50 KC.
Sampling and Distribution (either A/D or D/A): Simultaneous.	Sequential.

Accuracy (both A/D and D/A):
±0.05%, ±½ least significant bit
±0.01%, available on special order

Code (both A/D and D/A):
Binary or BCD.

Epsco SYSTEMS

A division of Epsco, Incorporated, 275 Massachusetts Ave., Cambridge 39, Mass., UNiversity 4-4950

CIRCLE 17 ON READER CARD

programmed tape punching

An electronic unit known as TAPE (Tape Automatic Preparation Equipment) produces punched tape at what

is claimed to be less than half the cost of conventional methods and in one-third of the usual time required for this operation. This savings is reportedly achieved by TAPE's ability to automatically edit, verify, duplicate and correct punched tape. The machine's logic circuitry analyzes word-group and keyboard commands, converting them to complete coded programs. A prototype system now in operation may be adapted to industrial and military applications. McDONNELL AIRCRAFT CORP., St. Louis 66, Mo. For information:

CIRCLE 200 ON READER CARD

programming systems

Three new programming systems will be available for users of the 1401 system. The three systems are COBOL, Autocoder and Input/Output Control System. The 1401 COBOL system will initially be available in the first quarter of 1962 for systems with core storage capacities of 8,000, 12,000 or 16,000 characters. A version for 1401's with 4,000 positions of core memory will become available during the second quarter of 1962. A 1401 will also require other standard units, such as magnetic tape drives, and special features to be able to handle COBOL. The Autocoder is now available, and ICCS will be made available in the third quarter of 1961. INTERNATIONAL BUSINESS MACHINES CORP., 112 E. Post Rd., White Plains, N.Y. For information:

CIRCLE 201 ON READER CARD

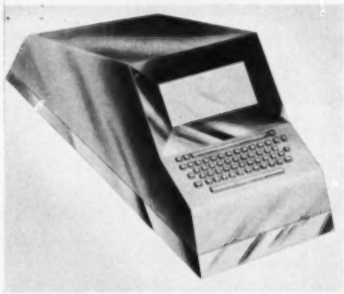
data punch

The Addressograph data punch is a portable unit which records data in standard punch card code directly on a tabulating card - at point of origin. Cards prepared by this punch can be fed into any data processing system without transcription or additional preparatory steps. It simultaneously interprets in human sensible imprint for verification and easy reference, data which is being punched into the card. ADDRESSOGRAPH - MULIGRAPH CORP., Cleveland, Ohio. For information:

CIRCLE 202 ON READER CARD

interrogator

The new 2502 interrogator can be used to send and receive detailed information from a remotely located computer. The entire unit measures 12 in. in length and width by 22½ in. in depth, and uses ordinary office power. The keyboard contains 40 standard alphanumeric keys, plus special transmit, clear and reset keys. Any 7 or 6 bit binary code can be used, with a bit rate of one megacycle. Character transmission rate is 15,800 characters per second. The 2502 also functions as a data entry device, permitting keyboard entry, with display verification to the

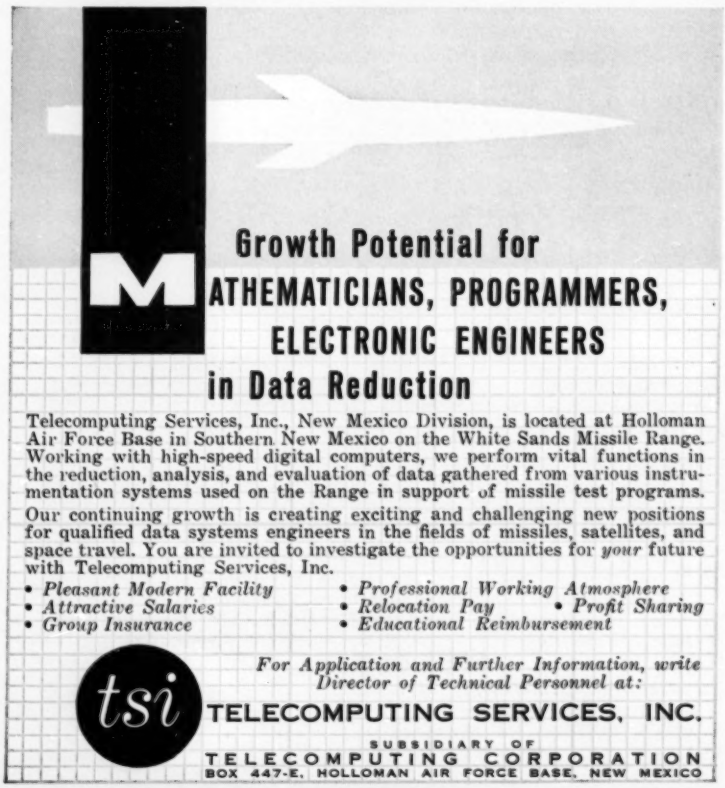


computer for adding to, modifying or updating stored data. INFORMATION PRODUCTS, 156 Sixth St., Cambridge, Mass. For information:

CIRCLE 203 ON READER CARD

computer diodes

Two series of silicon computer diodes are now available. 1N925 through


Growth Potential for
MATHEMATICIANS, PROGRAMMERS,
ELECTRONIC ENGINEERS
in Data Reduction
Telecomputing Services, Inc., New Mexico Division, is located at Holloman Air Force Base in Southern New Mexico on the White Sands Missile Range. Working with high-speed digital computers, we perform vital functions in the reduction, analysis, and evaluation of data gathered from various instrumentation systems used on the Range in support of missile test programs.
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CIRCLE 71 ON READER CARD

NEW PRODUCTS . . .

1N928 have low capacitance with reverse recovery times of 5 millimicroseconds. Types 1N789 through 1N804 are fast recovery silicon computer diodes, designed specifically for computer applications in which high switching speed and low leakage are criteria. Also available is a high conductance silicon glass diode, type 1N643A. PRINCETON ELECTRONICS CORP., P.O. Box 127, Princeton, N.J. For information:

CIRCLE 204 ON READER CARD

digital clock

A digital clock has been designed to serve as a long-duration data timer or as a date-time source for data processing equipment. The clock, a binary coded output of the day, hour, and minute is provided by contact closures permitting use of any logic voltage level from a data system. Employment

of stepping switches makes the date and time continuously and simultaneously available. A front panel visual readout is provided. In operation, the clock's basic timing pulses are formed from a cammicroswitch arrangement driven by an IRPM synchronous motor to produce the least significant minute count. ELECTRO-LOGIC CORP., 515 Boccaccio Ave., Venice, Calif. For information:

CIRCLE 205 ON READER CARD

dataplotter

A new digital plotter converts data from any digital computer system to graphic displays of engineering tests and problem solutions, sales, production and cost data. Able to accept analog as well as digital inputs, the 3100 provides accuracies up to 0.175 per cent of full scale on 11 x 17 in. X-Y plots of digital data and permits plotting up to 80 points per minute. The unit is equipped with transistorized

control circuitry, provisions for "off-board" origin, and is able to receive punched card, tape or keyboard input. ELECTRONIC ASSOCIATES, Long Branch, N.J. For information:

CIRCLE 206 ON READER CARD

filters

The PWI delta and gamma filters can be installed in the wiring of data processing equipment to eliminate electrical "feedback" or back circuits, and prevent interference with adjacent circuits. The filters permit currents to pass freely in the entry-to-exit direction but offer very high opposition to currents flowing in the reverse direction, and incorporate special components to provide buffering action for current blocking and arc suppression. PANELS WIRES INCORPORATED, 213 E. Grand Ave., South San Francisco, Calif. For instruction:

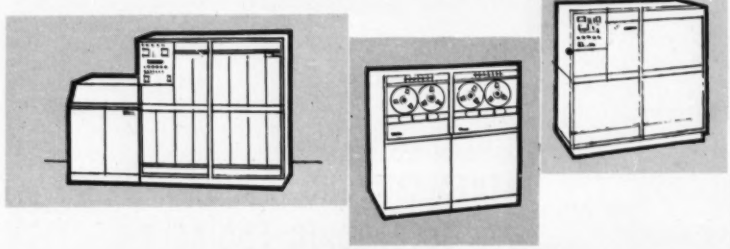
CIRCLE 207 ON READER CARD

digital readout

A small, lightweight, high-speed in-line digital readout presently in use in military systems now is available to other manufacturers. Total panel space required for the reader is .65 in. height and .50 in. from the center of one digit to center of adjacent digit. Assemblies with 3, 4, 5, and 6 digits are available. Maximum digit set-up time for all digits is .35 seconds. Binary

NEW ACOUSTICAL BATS
SILENCE COMPUTER SOUNDS

Available in 33-yd. rolls (72" wide) or in cut parts. Black or gray.



High-speed business machines just can't "think" without making some noise. Luckily, Western Felt has found the way to muffle that noise to a murmur.

It's a new vinyl-coated felt. Only ¼" thick, bats of this new noise barrier absorb 100% more sound at 600 cycles per second . . . and 300% more sound at 1000 cycles per second — compared to previously used ½" thick material. And — get this — it costs 26% less!

This new vinyl-coated felt bat by Western Felt is today's ideal sound deadener for business machines . . . computer equipment . . . and for many industrial applications. It's flameproof. Perforated vinyl prevents fibers from shredding. To learn how it can solve your sound problems, write for free samples and literature.

WESTERN Felt WORKS
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Chicago 23, Ill.
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MANUFACTURERS AND CUTTERS OF WOOL FELTS

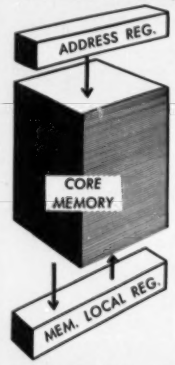
CIRCLE 18 ON READER CARD

From Honeywell:

A brief analysis of some of the basic terms used to compare computer performance

New claims, counter-claims, and comparisons of performance are being made by computer manufacturers every day. To help bring this welter of statistics into focus, Honeywell's Electronic Data Processing Division feels it necessary to define and briefly analyze a number of factors that are being considered in evaluating the relative performance of EDP Systems. Here are some of them:

MEMORY ACCESS TIME The memory device most widely used in electronic computers is the coincident-current magnetic core memory. It has three basic parts: An Address Register, a stack or array of magnetic cores, and a Memory Local Register.



When the Address Register receives information identifying a specific location in the core memory, the content of that memory location is transferred to the Memory Local Register, where it becomes available for processing.

Memory Access Time is the time it takes to perform this transfer.

MEMORY CYCLE TIME When information is transferred, the content of the memory location is destroyed. However, the information is still available in the Memory Local Register, where it can be, and usually is automatically restored to its original memory location. The time needed to restore this ininformation — Restoration Time — usually equals Memory Access Time.

Memory Cycle Time equals Memory Access Time plus Restoration Time. When new information to be stored is placed in the Memory Local Register for assignment to a memory location, it is inserted during the Restoration Time of a separate memory cycle and the Access Time of that cycle is generally not used.

Memory Cycle Time is often used to compare internal speeds of computers. For a valid comparison, the amount of information transferred during each cycle must be considered. For example, most small computers handle only one character at a time, while large systems often handle eight or more. Computers that utilize words of fixed length do not always handle a full word each cycle. Some handle half-words or quarter-words, and therefore take two or four memory cycles to transfer one computer word.

For comparative purposes, a more explicit expression of computer memory speed is the number of characters stored or retrieved by the memory in one second. On this basis, Honeywell 800 Electronic Data Processing System has an internal speed of 1,670,000 characters per second, far and away the highest speed in its price class. Furthermore, Honeywell 800 utilizes a separate control memory which often permits overlapping of internal operations, with consequent gains in speed.

INSTRUCTION TIME A fundamental measure of computer performance is the rate at which it carries out instructions. These instructions may contain one, two, three, or even four addresses. Honeywell EDP Systems, for example, use a three-address instruction which, on a conservative basis, is equal to about 2.2 one-address instructions.

Also, some types of instructions take longer than others, and when comparing computers it is important to know if instruction times quoted are for comparable operations. Various Honeywell 800 instructions are carried out at speeds ranging from 7,000 to 80,000 per second. The advertised speed of 30,000 operations per second is a conservative average.

ADD TIME The expression Add Time has generally been subject to extremely loose interpretation. For example, the Add Time of a three-address addition involves much more in the way of computer operation than the Add Time for a one-address instruction.

Add Time has been defined by some as the rate at which a succession of numbers may be totalled, and by others as the time the electronic circuits take to perform the actual addition, ignoring memory times. To be valid as a comparative function, the definition of Add Time should include the size of the numbers being added, the code they are in (binary or decimal), and whether or not the result involves a change in arithmetic sign.

OTHER CONSIDERATIONS There are, of course, several other factors that must be considered in evaluating or comparing the performance of electronic data processing systems. Among these are: use of internal checking, level of reliability, extent of simultaneous operations, and relative importance of certain special features. These and other subjects will be covered in future reports.

SEND FOR ADDITIONAL INFORMATION

In the meantime, if you would like more information about any or all of these subjects, just write to Honeywell EDP Division, Wellesley Hills 81, Mass., or Honeywell Controls Limited, Toronto 17, Ontario.

EMPLOYMENT OPPORTUNITIES

Opportunities exist for qualified professional personnel in all phases of EDP, from design to sales. If interested, please direct your confidential inquiry to our personnel director.

Honeywell

Electronic Data Processing

CIRCLE 19 ON READER CARD

HIGH PRECISION
TAPE DRIVE SPROCKETS
by LaVezzi
Made to your specifications
for
• ALL APPLICATIONS
• ALL SIZES AND FORMS
• IN ALL PRACTICAL MATERIALS
• IN SMALL OR LARGE QUANTITIES
Fine Finishes
Accurate Tooth Register
Perfect Tooth Size and Contour
YOUR QUOTE REQUESTS AND INQUIRIES INVITED
TEETH INTEGRAL WITH BODY
LaVezzi MACHINE WORKS
4635 W. LAKE ST., CHICAGO 44, ILLINOIS
MACHINE PARTS OF EXTREME ACCURACY SINCE 1908

CIRCLE 21 ON READER CARD

STORE...
CONVERT...
DELAY...
CONTROL...
TIME...
COUNT...
with this VERSATILE
10-STAGE
MAGNETIC REGISTER
This proven plug-in can wear at least six different hats in your digital systems. Draws less than flea-power from a single ±15% voltage source. Maintains 40:1 ONE:ZERO ratio. Cascades without limit. We mass-produce eleven standard designs up to 750 KC, hence can sell them at prices that dishearten competition. So reliable we use them ourselves!
Let us show you how to play the hat game with the SRA-10. A bundle of informative, inspiring literature awaits you. Write today.
di an
DI/AN CONTROLS, INC.
40 LEON STREET, BOSTON 15, MASSACHUSETTS
magnetic digital/analog systems and components

CIRCLE 20 ON READER CARD

NEW PRODUCTS . . .

coded decimal logic assures that the required digit is in position and provides a parity signal. Digit selection can be accomplished in serial or parallel fashion. COMPUTER SYSTEM LABORATORY, Litton Systems, Inc., Woodland Hills, Calif. For information:

CIRCLE 208 ON READER CARD

punched tape reader

The model 84, a new punched tape reader is suitable for "on-line" service in computer, communication and control applications. Data in the form of coded hole sets is photoelectrically read from punched tape and transformed to electrical output pulses. It is a self-contained unit. Nominal tape length is 500 ft. which provides a total punched tape capacity of approximately 60,000 data characteristics. COOK ELECTRIC CO., 2700 Southport Ave., Chicago 14, Ill. For information:

CIRCLE 209 ON READER CARD

computer diodes

Six new high speed diffused silicon mesa computer diodes with all glass microminiature packaging meet the environmental specifications of MIL-S-19500B. The diodes combine low leakage with fast switching speeds. The MA-4303 and MA-4304 diodes are rated at 10.0 milliamps at 1.0 volt forward and at -40 volts reverse. The MA-4307 and MA-4308 are rated at 30 milliamps at 1.0 volt forward and at .050 microamps at -75 volts reverse. They have an allowable junction temperature of 200 C and an operating temperature range from -61 C to -200 C. MICROWAVE ASSOCIATES, Burlington, Mass. For information:

CIRCLE 210 ON READER CARD

micro-module circuitry

The "789" series of sub-miniature encapsulated, transistorized digital and logic circuit modules are constructed of high reliability components. An entire series of digital and logic circuits is available, including binary counters, triggers, multivibrators, gates, inverters and flip-flops. The digital circuits are designed for frequencies in excess of 10 megacycles, with logic levels of OV and +6V. The binary counter produces output rise times of less than 40 nanoseconds, and can drive a 1500 ohm resistive load from each output at 10 megacycles. The series has been designed to meet continuous operating temperatures of MIL-E-5400 C, class 4, and the environmental requirements of MIL-E-5272 WALKIRT CO., 141 W. Hazel St., Inglewood, Calif. For information:

CIRCLE 211 ON READER CARD

SAVE COMPUTER TIME with the Moseley 575 Digital Magnetic Tape Plotting System

Tape can be written at 75 inches per second, read for recording at 3 inches per second, a 25:1 time-saving ratio that permits fast, efficient use of high-cost computers.

This complete data handling system plots information from magnetic tape prepared by the computer. Incorporating the Moseley Magnetic Tape Control Unit, Digital Converter, and a tape transport, the system stores and converts digital data for continuous plotting at 100 conversions per second to operate any Moseley Autograf Recorder.

Binary or binary coded decimal data may be accepted by the system, and a search mode is provided in which the data to be plotted is selected by means of identification codes written on the tape. A visual display is provided for check-out or calibration.

Accuracy of digital-analog conversion is ±0.1%; overall accuracy of the plotting system is ±0.2% of full scale; calibration stability of the precision reference supply is ±0.05%. Write today for details on this versatile system, moderately priced under $30,000.00

Also available a technical article on high-speed data plotting recently published in a national magazine. Write for Moseley Document 575-5.

AUTOGRAF *recorders*

Data subject to change without notice.

F.L. MOSELEY CO.

Dept. B-3, 409 N. Fair Oaks Avenue, Pasadena, California
MUrray 1-0208, TWX PASA CAL 7687 Cable MOCOPAS
Field representatives in all principal areas

6789

CIRCLE 22 ON READER CARD

new DATAMATION literature

The following literature was published by Philco Corp., Philadelphia 34, Pa.

DIFFERENTIAL EQUATIONS: A report describes a program for the solution of a system of N first order differential equations with error control. The report includes a standard routine description and flowcharts.

CIRCLE 260 ON READER CARD

MATRIX MANUAL: A new manual describes the transportation of matrix A and the storing of the transposed matrix in a separate area, B.

CIRCLE 261 ON READER CARD

PREPARATION BOOKLET: A booklet describes what to do before installing a computer system. It is in non-technical language and describes system analysis, specifications, design and the full operation of the computer.

CIRCLE 262 ON READER CARD

INPUT EDIT, OUTPUT EDIT: Input edit and output edit associated with linear programming routines is described in a newly prepared report.

CIRCLE 263 ON READER CARD

BUILDING BLOCK: A two-page bulletin describes and illustrates the model c/o6p/s/O-O/IN stored program analog computer building blocks. It is designed to handle six pairs of operational plug-in amplifiers. Specifications and diagrams accompany the text. EMBREE ELECTRONIC CORP., 993 Farmington Ave., West Hartford 7, Conn. For copy:

CIRCLE 264 ON READER CARD

THIN FILM MEMORY: A six-page publication deals entirely with the subject of thin film memory. It describes the behavior of the memory elements, operating characteristics and a description of different types. Application, ordering accessories and electrical information is offered. The booklet is supplemented with photos, and diagrams. BURROUGHS CORP., Plainfield, N.J. For copy:

CIRCLE 265 ON READER CARD

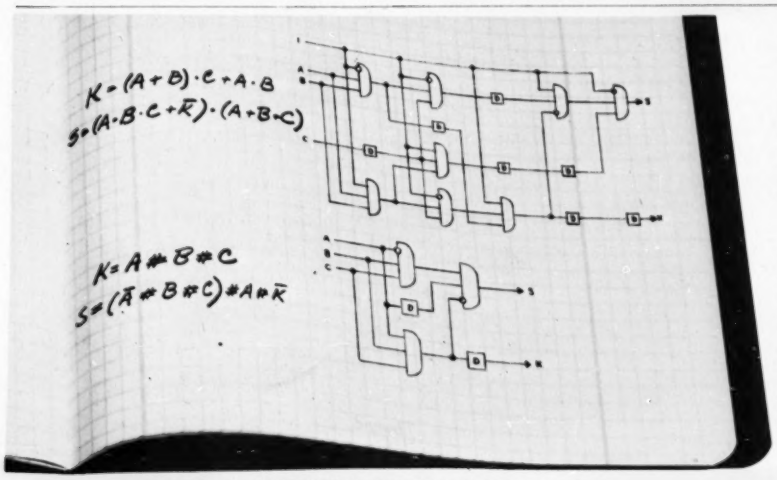
APPLICATION REPORT: A three-year report on the results of the work of a G-15 computer at American Viscose Corp. is now available. Major applications are statistics, curve-fitting and correlations. Special uses include the search of spectra files on magnetic tape, and nuclear resonance spectroscopy. BENDIX CORP., Computer Division, 5630 Arbor Vitae St., Los Angeles 45, Calif. For copy:

CIRCLE 266 ON READER CARD

MICROWAVE SYSTEM: A 12-page bulletin describes the LMR20 6 kmc microwave system. The system consists of radio, multiplexing and the necessary antennas, towers, buildings, etc. for each individual station. The publication includes photographs, charts and diagrams. LYNCH COMMUNICATION SYSTEMS INC., 695 Bryant St., San Francisco 7, Calif. For copy:

CIRCLE 267 ON READER CARD

PUNCHED TAPE READER: A complete description of the type RA-1656 punched tape reader is contained in a bulletin now available. The unit can read punched tape at 1500 characters



The binary adder stage produced in conventional design (top) has been reduced and simplified through Majority Logic Design to the diagram and formula at the bottom. Discovered and formulated in the Remington Rand Univac Mathematics and Logic Research Department, Majority Decision Logic is a new logical algebra, which opens new and interesting possibilities for the reduction in the number of logical elements in computer design.

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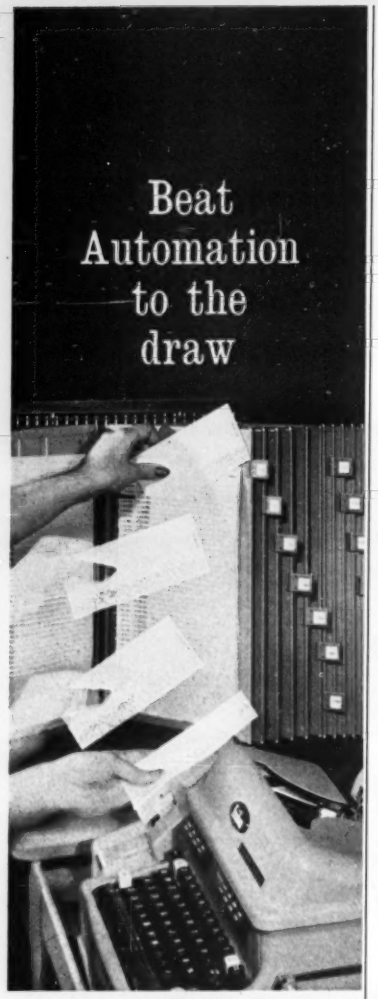

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CIRCLE 268 ON READER CARD

G-20 REPORT: This report describes how the G-20 uses multiple regression analysis and linear programming to provide management with data for improved control and decision making. The report also describes the application of linear programming to production scheduling. BENDIX COMPUTER DIVISION, 5630 Arbor Vitae St., Los Angeles 45, Calif. For copy:
CIRCLE 269 ON READER CARD

ALPHA-NUMERIC DISPLAY: A new two-page bulletin B262, contains information on solid state alpha-numeric display. Included in the publication is a description of the electrical operation and display properties. Illustrations cover operational block diagrams, modular printed board arrangement, segment configuration and alpha-numeric gate line coding. ROBOTOMICS CORP., 2422 E. Indian School, Phoenix, Ariz. For copy:
CIRCLE 270 ON READER CARD

DATA TRANSMISSION SYSTEMS: A brochure describes the transfer of data from offices, distribution points and branch plants to a centralized computer. Several combinations of terminals are available. STROMBERG-CARLSON, 1400 N. Goodman St., Rochester 3, N.Y. For copy:
CIRCLE 271 ON READER CARD

TAPE READER BULLETIN: The use of chopped reflected light to achieve reliable tape reading and stability of operation by a new photoelectric tape reader is described in bulletin PTR-7. OMNITRONICS, INC., 511 N. Broad St., Philadelphia 23, Penna. For copy:
CIRCLE 272 ON READER CARD

SOVIET TRANSLATIONS: Translations of a Russian book review and two Russian articles on computers have been compiled in a volume discussing foreign developments in machine translations and information processing. The book is one of nine translations of Soviet computer literature just released to science and industry through the Office of Technical Services, Business and Services Administration, U. S. Department of Commerce, Washington 25, D.C. The translations are:

60-31877 FOREIGN DEVELOPMENTS IN MACHINE TRANSLATION AND INFORMATION PROCESSING. USSR. October 1960, 21 pages, 75 cents.

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Said Gaspard de Coriolis: *"A particle which is subject to no forces in a rotating coordinate system experiences a radial acceleration and a tangential acceleration."*

It was around 1840 that Coriolis discovered what has since become known as the Coriolis Effect. He noticed objects above the earth tend to rotate relative to the earth's rotation . . . to the right in the northern hemisphere, to the left in the southern.

The Coriolis Effect is in force in outer space, too. If a space vehicle is rotated in order to establish artificial gravity, the necessarily short radius of the rotation causes a Coriolis force. This creates orientation problems for a human occupant. To eliminate this difficulty, a scientist at Lockheed Missiles and Space Division conceived the idea of connecting the vehicle to an auxiliary fuel tank by a half-mile-long cable. Thus, if the whole system is then rotated at a reduced speed around its center of mass gravity, the longer radius greatly minimizes the Coriolis force. Right now—on the drawing boards at Lockheed—is an enormously advanced space vehicle system which utilizes this concept, in addition to many others.

Fortunately, natural laws are about the only restrictions which circumscribe scientists and engineers at Lockheed Missiles and Space Division. The climate in Sunnyvale and Palo Alto, on the San Francisco Peninsula, is close to perfection. The creative atmosphere—the opportunity to work on such important projects as the DISCOVERER and MIDAS satellites, the POLARIS FBM, or even more advanced concepts such as the space system cited above—is the dream of the creative engineer.

Why not investigate future possibilities at Lockheed? Write Research and Development Staff, Dept. M-11C, 962 West El Camino Real, Sunnyvale, Calif. U.S. citizenship or existing Department of Defense industrial security clearance required.

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TECHNOLOGY CENTER, CHICAGO 16, ILL.

CIRCLE 73 ON READER CARD

NEW LITERATURE . . .

60-41693 INPUT AND OUTPUT OF INFORMATION IN HIGH-SPEED DIGITAL COMPUTERS. October 1960, 42 pages, $1.25. Translation of an article in Avtomaticheskoye Upravleniye i Vychislietel'naya Tekhnika, Moscow, 1958. N. V. Trubnikov.

60-41030 TsEM DIGITAL ELECTRONIC COMPUTER. July 1960, 28 pages, $1. Translation of an article from Problemy kibernetiki, No. 1, Moscow, 1958. G. A. Mikhalov and others.

61-11013 CYBERNETICS AND MAN. November 1960, 4 pages, 50 cents. Translation of an unsigned article from Priroda, Moscow, Vol. XLIX, No. 8, August 1960.

60-41267 SUPERCONDUCTIVITY AND CYBERNETICS. August 1960, 11 pages, 50 cents. Translation of an article from Priroda, No. 2, Moscow, February 1960. A. N. Zimarev and V. Ya. Kontarev.

60-41724 CONCERNING THE AUTOMATION OF PROCESSING OF EXPERIMENTAL DATA IN INVESTIGATING THE IRREGULAR IONOSPHERE. November 1960, 20 pages, 75 cents. Translation of an article from Vestnik Moskovskogo Universiteta, Seriya III, Fiz. Astron., Moscow, 1960, No. 1. V. D. Gusev and T. A. Gaylit.

60-41585 THE USE OF THE M-2 ELECTRONIC DIGITAL COMPUTER (BRIEF REPORT) October 1960, 17 pages, 50 cents. Translation from mono. 1959. A. L. Brudno and Yu. A. Lavrenyuk.

60-41262 PRINCIPLES OF DESIGNING, CONTROLLING MATHEMATICAL MACHINES ON THE BASIS OF GENERAL PURPOSE HIGH SPEED DIGITAL COMPUTERS. September 1960, 31 pages 75 cents. Translation of mono. Moscow, 1958. V. A. Zimin.

60-41270 SYMBOLIC PROGRAMMING FOR THE ELECTRONIC COMPUTER OF THE ACADEMY OF SCIENCES, LATVIAN SSR. October 1960, 15 pages, 50 cents. Translation of Akademiya Nauk Latviyskoy, USSR (Riga) Isvestiya, 1958. Ye. I. Arin' and M. A. Shneps.

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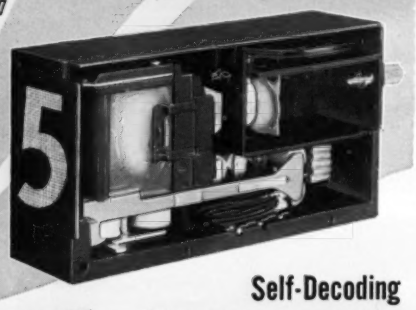

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CIRCLE 28 ON READER CARD

new dp system

IBM ANNOUNCES THE 7072

IBM's 7072 is the newest data processing system announced by that firm "for commercial and scientific applications which do not require the high input/output speeds of the 7074," according to a recent release. Actually, the 7072 is a smaller, less expensive version of the 7074 having two fewer computer modules (four instead of six) and leasing for $19,825 (compared to $29,300).

The 7072 is available only with off-line equipment (the 1401) and is tape oriented. The lease price noted above includes the 1401 and six 7030 tape units. The 7072 utilizes the same arithmetic and cpu modules as the 7074.

Either 5,000 or 10,000 ten-digit decimal words of core storage are available for the 7072. As an optional feature, memory can be expanded in modules of 5,000 to a total of 30,000 words. Binary recorded information from magnetic tape may be read directly into the 7072 which converts it, through a program subroutine, into decimal.

Fixed point add/subtract speed (six digits) is 12μ; multiplication (10 digit x 10 digits) – 64μ (avg.); division (20 by 10) – 94μ (avg.). Floating point (built-in and standard) speeds are add – 20μ; subtract – 26μ; multiply (8x8) – 64μ (avg.) and division (8 digit avg. quotient) – 95μ.

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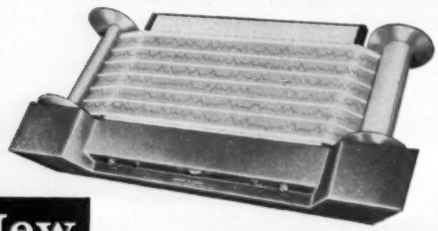

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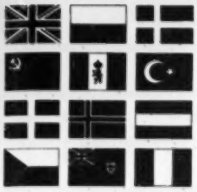

DATAMATION *abroad*

NORWAY

Freia A/S of Oslo has become the first industrial firm in Norway to introduce a computer for data processing. The firm is renting an IBM 305 Ramac for the purpose of invoicing, perpetual inventory, sales statistics, customer accounting, and debt collecting surveys.

ENGLAND

The British Ministry of Aviation has placed an order with Elliott Brothers Ltd., London, for a 502 computer to be included in experimental air traffic control equipment scheduled for installation in the near future. The 502 will be the central data processing unit, and also will be incorporated in the development of training simulators.

RUMANIA

The third electronic computer made by the Institute of Nuclear Physics of the Rumanian Academy of Sciences was recently put into operation. The computer, Cifa-3, was installed at the Bucharest C. I. Parhon University for use in research and training.

ITALY

An IBM 7070 is now in operation at the electronic center of the Italian Radio Television network in Turin. This is the first radio-TV system in the world, an official stated, to use a computer for its administration, accounting and statistical operations. It is also the first 7070 to be put into operation in Italy.

U.S.S.R.

V. A. Bugayev, director of the Central Weather Forecasting Institute in Moscow, stated recently that it is now possible to use computers for weather forecasts 24 hours in advance. The Institute has drawn up a system of equations for computing the weather conditions several days ahead. Methods for forecasting for each coming month were also being worked on. Mathematical methods would be used more widely for long term forecasts.

U.S.S.R.

"French machines are more modern and obey the newer principles than the classical machines which seem to be obsolete, and they differ from large Russian computers as they are more easily usable for the needs of the Russian economy," stated V. Veise, after viewing the Bull exhibition in Moscow. Two contracts were signed in the USSR as a result of the display. A Gamma Drum will be delivered to the USSR Academy of Sciences. The exhibition was termed a success as it drew over 13,000 specialists of electro-mechanical and digital computing.

U.S.S.R.

Seventy Soviet satellite tracking stations, located throughout the USSR, relay their information to a central computer center, Alla Masevick, vice chairman of the Astronomical Council of the USSR Academy of Sciences revealed recently. By January, 1961, over 90,000 observations had been received at the computer facility, including 37,000 from non-Russian countries.

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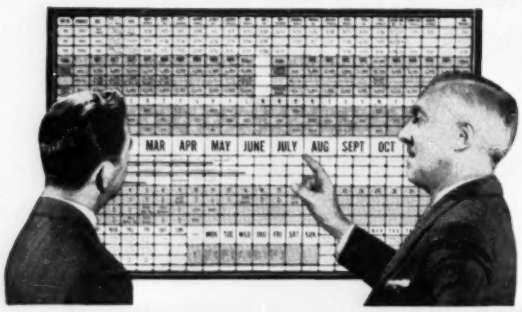

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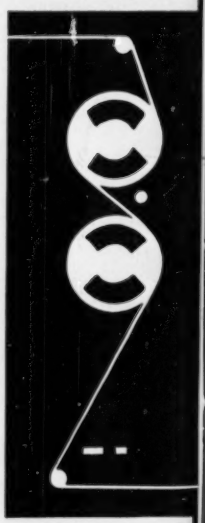

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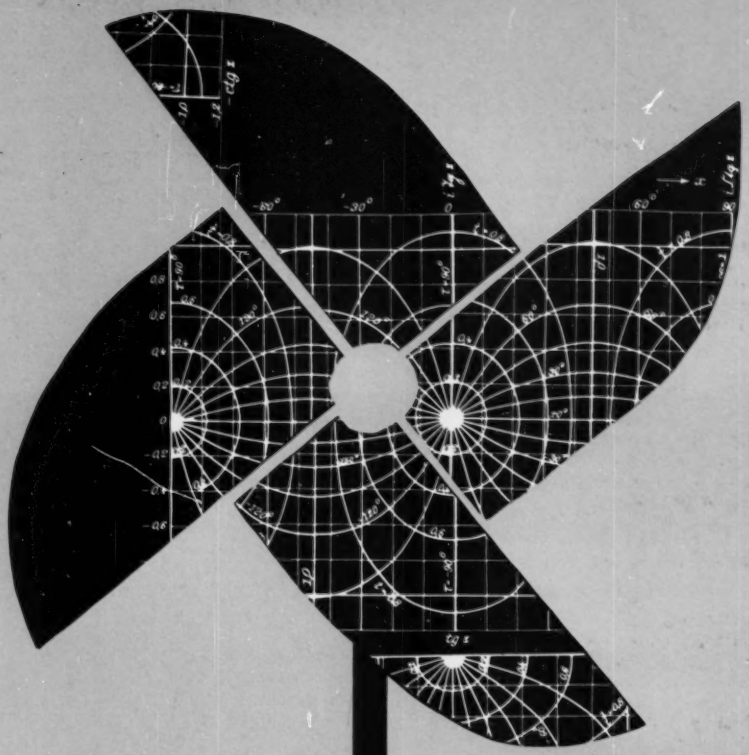

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